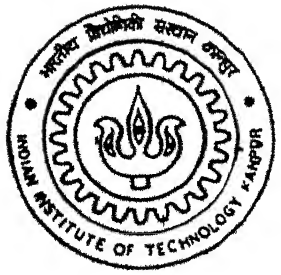
STUDIES ON FAST INFRARED INDOOR OPTICAL WIRELESS LINKS

By

NISHA KURUVILLA



DEPARTMENT OF ELECTRICAL ENGINEERING

Indian Institute of Technology Kanpur

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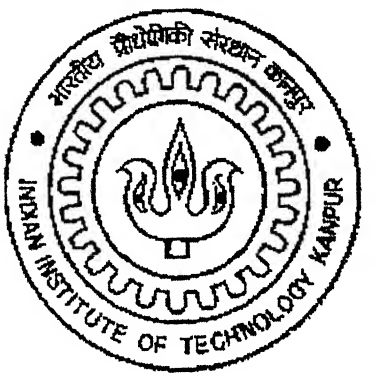
A Thesis Submitted
in Partial Fulfillment of the Requirements
for the Degree of
Master of Technology

by

NISHA KURUVILLA



to the

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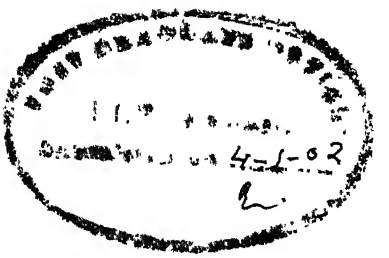

CERTIFICATE

This is to certify that the thesis work entitled **"STUDIES ON FAST INFRARED INDOOR OPTICAL WIRELESS LINKS"** by Ms. Nisha Kuruvilla, Roll No. Y010424 has been carried out under my supervision and the same has not been submitted elsewhere for a degree.

January 2001

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ABSTRACT

In recent years Wireless Infrared (IR) communication systems are being used widely to provide portable data communication at low cost. IrDA standards have emerged in order to meet the growing demand in this field. This thesis deals with the study of fast infrared indoor (FIR) indoor optical wireless and the design and implementation details of an experimental IrDA compatible FIR optical wireless link. The experimental IrDA compatible FIR link achieved a link length of 16cm. 4Mb/s data is encoded with the help of a 4PPM encoder and wrapped into a packet form along with preamble, beginning of frame and end of frame pattern with a FIR data wrapper. The FIR data wrapper for 256 chips, is implemented with the help simple discrete components. These data were transmitted using a low cost IR LED as the source. The receiver is PIN diode based, with a JFET as the front-end amplifying device. The clock from the received signal was recovered back with the help of a digital PLL. The encoded data was decoded back with the help of a 4PPM decoder.

ACKNOWLEDGEMENTS

All my gratitude for the successful completion of this project goes to Dr. Joseph John, without whose help, guidance and supervision this project would not have seen light. His constant support and ready availability at all times made me complete this work on time. Mrs. Neena Joseph deserves special mention for the encouragement and moral support she gave me.

I am thankful to the authorities of my parent organisation IHRD for providing me this opportunity for doing M.Tech under QIP.

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Let me take this opportunity to express my gratitude to my parents and in laws for their constant encouragement, moral support and patience.

I would like to thank Mr. S. K. Kole and the staff of the PCB lab for making the PCBs on time, and of course to Ram Birbal for helping me with the soldering and Sanjay for all the lab assistance rendered.

Thanks to all my Christian friends who supported me through their prayers. I am grateful to my friends Deepa, Swamna, Dawnee, Rajanji and family for their excellent company during my stay at IITK.

Last but not the least my special gratitude to my better half, Vino and our kids Jevin and Jerry for silently bearing the burden of my studies at IIT Kanpur.

Nisha Kuruvilla

To

My Lord and my God

CONTENTS

CHAPTER 1
INTRODUCTION

1.1 INTRODUCTION

We are living in a bandwidth-hungry, data-centric world. Current data traffic growth is in triple digits. Tomorrow's bandwidth demand will be even greater. Businesses need infrastructure to handle the increasing demands of data, video, and voice traffic. And in this competitive world Service Providers need to find ways to differentiate themselves from their competition. They need to be able to introduce new revenue-generating solutions, fast, today not tomorrow. To keep ahead of the competition, service providers need a scalable, optical service platform that is cost-effective and creates flexibility and the opportunity to successfully compete. The ideal solution for delivering bandwidth hungry services reliably, securely, and scalable is an end-to-end optical transport network solution [6].

Mobile professionals are using a wide class of computing devices and peripherals such as laptops, palmtop computers, personal digital assistants and simple function devices like electronic business cards or phone dialers. The emergence of portable information terminals in work and living environment is accelerating the introduction of wireless digital links and local area networks. Portable terminals should have access to all the services that are available on high speed wired network. The advantages of wireless networks over wired network are their flexibility and lower cost. Traditionally, radio frequency transmission was used in wireless applications. However, the RF spectrum is so congested that it is very difficult to accommodate new high bit rate applications. The best alternative is to use optical wireless network. Since optical systems are less complex in implementation and have no spectrum license requirements, they provide a possible solution. The desire for inexpensive, mobile high-speed links, has motivated interest in infrared wireless communication. By 1993 several commercial products were available with this capability. The objective for the free space LAN system is to obtain the above advantages as well as also for the first time to provide seamless full bit rate capacity, and

Ethernet integration. Basically, optical wireless systems can be classified into two, viz. indoor systems and outdoor systems.

1.2 INDOOR OPTICAL WIRELESS SYSTEMS

The use of an optical wireless network for indoor applications offers numerous advantages over the equivalent RF wireless network. The optical energy can typically be contained within the room communication environment, thus virtually eliminating the problem of interference generated by neighboring users while offering a degree of security at the physical level. The same transmission equipment and optical wavelength can be reused in other parts of the building, thus offering spatial diversity and it is almost immune from signal fading As such, indoor infrared communication has recently received much importance in view of the increased data and mobility requirements of users in both computing and communication applications. Indoor IR systems comes in the category of short distance systems Indoor systems have the major advantage that the, distance involved are much less than the outdoor systems. There are four types of indoor optical wireless systems, viz Point–to–point links, Tele-point Systems (point-to-multipoint), diffuse systems and tracked systems [5]. Basic optical wireless systems is divided into four system topologies and they are line of sight (LOS), wide line of sight (WLOS) or cellular, diffused and tracked.

1.2.1 POINT- TO- POINT LINKS

Point- to- point links can be indoor or outdoor type. Outdoor short distance systems are used to deliver high capacity links between neighboring buildings, enjoy the luxury as do long distance systems, of utilizing a high power Class 3B emitter since system is located away from people. So a good power budget can be obtained using relatively simpler components. This combined with low atmospheric loss, means that a higher free space loss can be tolerated in return for the convenience of a larger beam diameter at the receiver. Usually by utilizing this mode we can transmit data of 1Gb/s over 40m distances. Indoor point- to- point systems do not differ from the outdoor variety in their operating principles, however their designs are invariably very different and it will be discussed in detail in later section of the report [5,6].

1.2.2 TELE-POINT SYSTEMS

Indoor applications being fundamentally confined to short distance spans are uniquely appropriate to optical wireless systems that utilize wide diverging beams rather than the narrow beams of point-to-point systems. Such systems are referred as tele-point systems Here each cell is created by a tele-point base station can be shared by as many users as can sensibly be accommodated within the cell. Cell diameter can vary from 0.5m to 10m. The larger cells might be deployed in open offices, libraries etc and smaller cells are for single user, such as a telephone booth [5].

1.2.3 DIFFUSE SYSTEMS

In this group of systems the beams are radiating over a wide angle, and are also allowed to reflect off surfaces and objects in the vicinity such as walls, ceilings, floor and furniture. Here the field of view is widened to such an extent that the line of sight as well as reflected light can be detected with same ease. This arrangement also allows roaming to some degree. The main disadvantage is reduction in capacity due to diffused transmission compared with point-to-point systems [5].

1.2.4 TRACKED SYSTEMS

In many indoor applications it is desirable to deliver capacities more than 10 Mb/s and also provide facility for some amount of roaming. This necessitates the use of a narrow beam from a base station located in the ceiling of the room illuminating the mobile unit. Usually laser beams are used as emitters and in order to remain class 1 eye safe they are operated at low power levels. This spotlight beam is steerable and so it can track the mobiles as they move around the coverage area. To date the beam steering is achieved by steerable optics. The beams are reused as the user enters and leaves the cells, the maximum number of users at any time being determined by the number of simultaneous down beams that the base station can produce. An experimental system with a data rate of 155Mb/s has been demonstrated using this concept [5,6].

1.3 AIMS AND OBJECTIVE OF PRESENT WORK

Aim: -The aim of the present work is to study indoor FIR (Fast Infrared) systems and to design and implement an experimental indoor FIR wireless link.

Objective: The objective of the work encompasses the following:

(a) Study of indoor FIR systems

(b) Design an experimental Fast Infrared (FIR) optical transmitter and receiver based on IrDA standard.

1.4 THESIS LAYOUT

Chapter 2 of the thesis gives a detailed review of indoor point-to-point IR links. An overview of IrDA, its various layers, and data formats are also given. Chapter 3 is devoted to the design of an experimental indoor point-to-point link based on FIR standard by IrDA. Chapter 4 gives details of the hardware implementation of the IrDA compatible FIR link. The thesis is concluded in chapter 5 with conclusion and suggestions for further work. A detailed list of references used in our work is given at the end.

CHAPTER 2

REVIEW OF INDOOR POINT- TO- POINT OPTICAL WIRELESS SYSTEMS

A review of indoor point-to-point optical wireless communication systems is discussed in this chapter. IrDA standard for indoor systems is also described.

2.1 INTRODUCTION

The commercial exploitation of optical wireless systems is at present getting wider attention. The increasing demand for access to a wide band network by the end users will encourage the industry to move into and invest in a big way in optical wireless systems. The next generation of PCs will have built-in optical transceivers. The emergence of portable information terminals in work and living environment is accelerating the introduction of wireless digital links and local area networks. Portable terminals should have access to all the services that are available on high speed wired network The advantages of wireless networks over wired network are their flexibility and lower cost. Traditionally, radio frequency transmission was used in wireless applications. However, the RF spectrum is so congested that it is very difficult to accommodate new high bit rate applications. The best alternative is to use optical wireless network [4]. Since optical systems are less complex in implementation and have no spectrum license requirements they provide a very good alternative. The desire for inexpensive, mobile high-speed links, has motivated recent interest in infrared wireless communication.

2.2 POINT- TO- POINT INDOOR IR SYSTEMS

Indoor point- to- point systems comes under the category of line of sight systems or directed links, since they employ directional transmitters and receivers, which must be

aimed in order to establish the links. This link design maximizes the power efficiency and minimizes the multi-path distortion. As there is no mobility, the beam aperture angle and field of view (FOV) of the emitter and the receiver can be reduced and thereby power losses are minimized. This also results in low transmit power requirements Indoor point-to-point systems do not differ from the outdoor variety in their operating principles, however their designs are invariably very different. One of the major requirement is that light emitter used must be class 1 eye safe, hence the optical source used normally is an LED [5]. This in turn limits the capacity to typically a few Mb/s. One of the advantages of indoor systems is that they do not require water proofing unlike their outdoor counterparts Indoor systems have another advantage that they do not suffer the derogatory effects of a multipath environment [6]. Also the receiver in this system does not require a large field of view and so the effective gain of the concentrator can be exploited to improve the link budget [27]. The main drawback is the lack of mobility and susceptibility to blocking by personnel. So transmitting LEDs are usually positioned high on posts to avoid shadowing. Very narrow beam also causes pointing problems. The beam-width should be so chosen that any inexperienced operator should be able to aim the transmitter lens towards the receiver unit by hand adjustments. Also normal vibration or inadvertent impacts on the desk should not misalign the beam a major fraction of its beam width. The advantages of indoor point-to-point systems over indoor diffused systems are:-

- they require less optical power for reliable communication
- they do not suffer from extensive multipath, and
- they can handle bi-directional communication better.

Hence higher data rates can be achieved by point-to-point systems compared to diffused systems. This method is typically used for the applications in which the terminals are relatively fixed such as desktop computers in an office. The basic block diagram of the transmitter in a point-to-point indoor IR system is shown in Fig. 2. 1 and the receiver in Fig. 2.2.

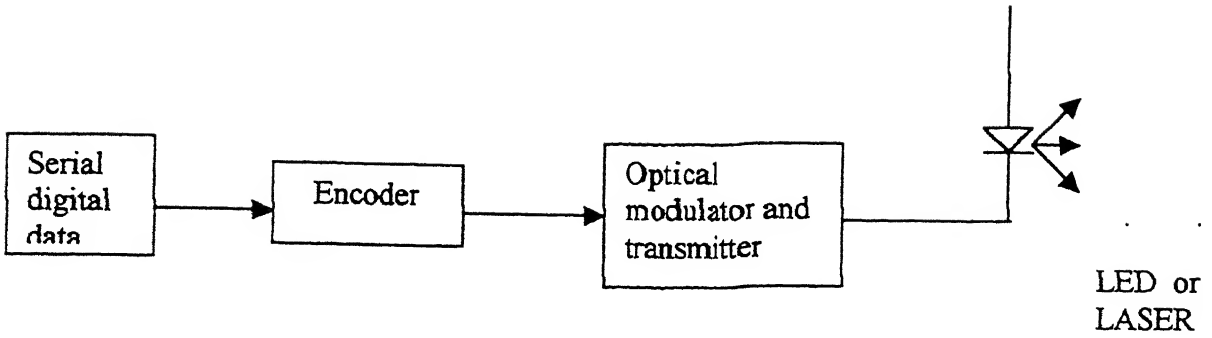


Fig. 2.1 Block Diagram Of Point-To-Point Optical transmitter [1]

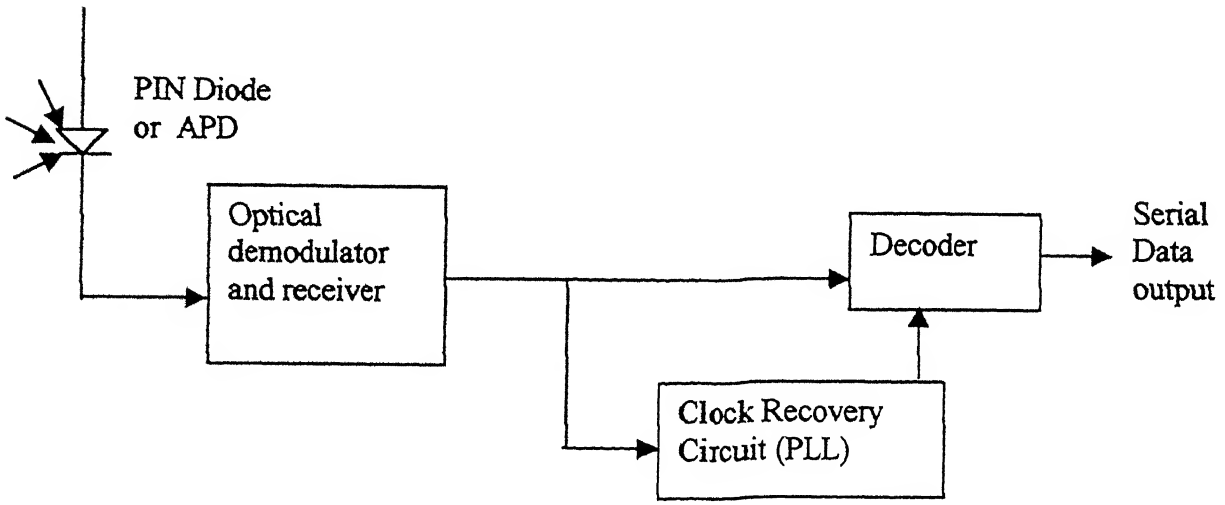


Fig: 2.2 Block Diagram Of Point-To-Point Optical Receiver

2.2.1 ENCODER / DECODER FOR INDOOR SYSTEMS

The serial digital data from the information source should be suitably encoded being transmitted as IR pulses and decoded back at the receiver. Non- return-to-zero, on-off –keying (NRZ-OOK) is widely used due to its simplicity and excellent bandwidth capability [5]. But the spectra of NRZ does not contain discrete spectral component for a truly random data, so either some non-linear clock recovery scheme is required at the

receiver or line coding must be used. In NRZ coding the output remains at the same level for the entire bit period and can stay at one level for multiple bit periods. This is not optimal for IR data transfer since a continuous string of bits could turn on the LED transmitter for an arbitrarily long time. Since IR receivers contain a high pass filter to remove background daylight, encoding of the data is required to ensure that long strings of zeros or ones are not lost in transmission. Also if long strings of ones and zeros are present in the data the power of the LED will have to be reduced to prevent its damage. But reducing the LED power will put a limit on the working distance achievable Thus the encoding scheme should help to increase peak to average ratio so as to obtain better signal to noise ratio at the receiver. The various encoding schemes used in Indoor IR transmissions are RZ (return to zero), NRZ L-level PPM and DPPM.

In the RZ scheme either zero or one will be transmitted as a pulse with $\frac{n}{m}$ bit duration (where n < m). In RZ signaling, the spectra have discrete spectral components at the bit rate transitions, making clock recovery with a PLL (Phase locked loop) possible. If RZ scheme uses pulses of 50% duty cycle then its bandwidth efficiency is half that of NRZ. This code is power efficient since infrared light is only transmitted for either zero or one. RZ scheme is generally used for IrDA systems with data rates 2400 bits/s to 4 Mb/s (i.e. in SIR and MIR systems).

Another encoding method is L–level pulse position modulation (L–PPM) which is also widely used. In an L–PPM scheme, M bits of data are conveyed by a single pulse in one of $L = 2^m$ positions. L-PPM offers improved bandwidth efficiency compared to NRZ schemes [3,6]. It is extremely popular in low bit rate commercial applications. L-PPM is the recommended encoding scheme in IrDA compatible links above 4Mb/s. The tall narrow pulse has better signal to noise ratio performance than a wide pulse. PPM has many features that make it attractive for use on the free space optical channel. One of the major features is sparseness of the code. Sparse code allows high peak powers to be employed for set chips while maintaining a reasonable average power. The eye safety rules stipulate a maximum average optical power and LED tends to be average power limited at moderate duty cycle.

PPM also contains significant and regular timing content, which facilitate synchronous clock recovery using a PLL. One of the interesting features of PPM is that it provides important ramification in the choice of end limiters and is also able to detect code errors. Higher orders of PPM give lower duty cycle and theoretically greater signal to noise ratio. 3PPM provides maximum bandwidth efficiency, but is not recommended in practical systems. Since the fastest bright LEDs have a rise time of around 40ns, and rise time of LED is proportional to pulse width, the use of higher order PPM at data rate above 4Mb/s become impractical [24]. The decision to adopt the order of four for the PPM was motivated by knowledge of the range of duty cycle over which LEDs are peak power limited, the rise and fall time of available LEDs. 4 -PPM appears to be a good compromise because the bandwidth occupancy is only twice that of NRZ OOK (or equivalent to 50% duty cycle) whilst offering a 4dB improvement in power efficiency [6]. 16PPM can offer power efficiency improvement on the order of ≅ 8dB. But the required bandwidth is increased by a factor of four. It remains to be seen whether PPM will find application at high bit rate application (i.e. above 50Mb/s) due to the increased bandwidth requirement as this will increase the f^2 noise in the pre-amplifier [6].

The other encoding schemes used are, all PTM (pulse time modulation) techniques such as PWM (pulse width modulation), PIM (pulse interval modulation), PIWM (pulse interval and width modulation), PFM (pulse frequency modulation), DPPM (differential pulse position modulation) etc and PPM in conjunction with CDMA techniques. In DPPM each symbol is transmitted as a pulse of one time-slot duration, located in the k-th slot after preceding pulse, where k is determined by the data word to be transmitted. As the frame length is variable DPPM offers improved transmission capacity over PPM. DPPM has shown higher cutoff rate than PPM for a certain range of physical parameters like power efficiency and lower hardware complexity than PPM. Some examples of encoding commonly used are shown below in Table 2.1 and Fig.2.3.

Source Bits	Corresponding 4 -PPM (nominal mapping)	Corresponding 4 –DPPM (nominal mapping)	Corresponding 4PPM (reverse mapping)
00	1000	1	0001
01	0100	01	001
10	0010	001	01
11	0001	0001	1

Table 2.1 Examples of Mapping Between Source Bits and Transmitted chips for 4PPM and 4-DPPM

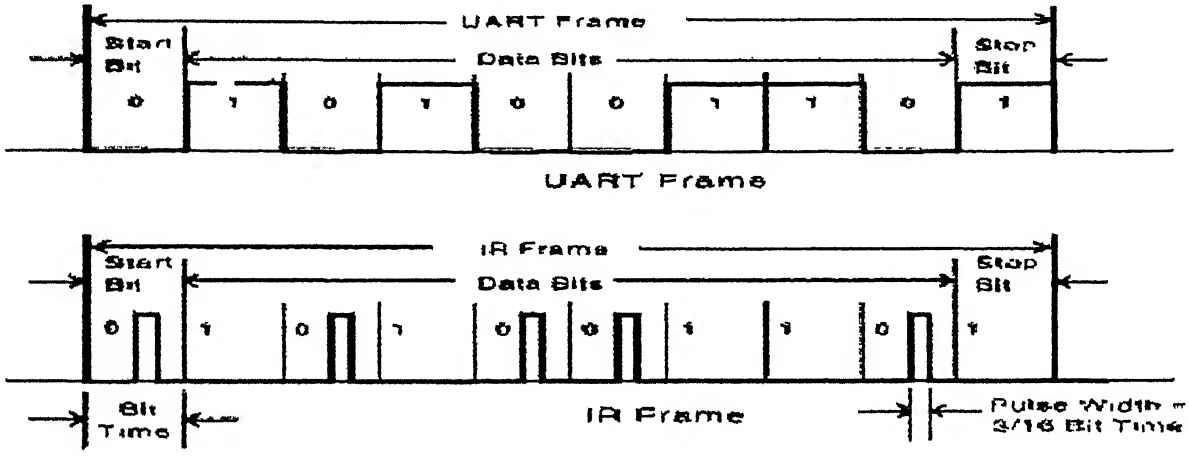


Fig 2.3 Example of 3/16 (n/m) RZ encoding scheme [7]

2.2.2 OPTICAL MODULATOR AND TRANSMITTER

In order to transmit information via wireless medium, it is necessary to modulate a property of light with the encoded information signal. This property may be intensity, frequency, phase or polarization (direction) with either digital or analog signals. The choice is based on the characteristics of medium of transmission, optical sources and optical detectors. Coherent optical transmitters modulate the phase or frequency of the optical carrier and coherent (heterodyne) optical detectors add light from a local laser to the received light wave as part of detection [1,27]. Since the background illumination has a broad spectrum, its effect on coherent detection is almost negligible. However, tracking the

light attributes like direction and its polarization and to match them with the local signal is difficult. So coherent detection is not feasible in non-directed links. Today's practical optical wireless communication systems tend to dictate some form of intensity modulation of the source as coherent optical systems are yet to be exploited in practical systems. Hence intensity modulation (IM) of the optical source and direct detection (DD) at the optical receiver remains the major strategy.

Intensity modulation is easy to implement with the electro-luminescent sources available at present (LEDs and injection lasers). These devices, especially injection lasers, can be directly modulated simply by varying their drive currents at rates up to several gigahertz Intensity modulation may be used with both digital and analog signals. Analog intensity modulation needs comparatively large signal to noise ratio and therefore it tend to be limited to systems capable of relatively large signal to noise ratios. Optical wireless systems generally use digital intensity modulation.

Optical sources are chosen depending on the requirement of optical power, rise and fall times, stability, field of view etc. In choosing the transmitter for a high speed, non-directed link, laser diodes have many advantages over light emitting diodes, viz., laser diodes can be modulated faster, they convert electrical power to optical power more efficiently and they can emit more optical power. Also the narrow line width of a laser diode, in comparison to an LED, allows the receiver to use a narrower optical filter thus rejecting background light. However, for indoor applications laser sources pose a potential safety hazard, as they are point source emitters. LEDs on the other hand are large area emitters and thus can be operated safely at relatively higher powers [28]. They are therefore the preferred emitter for most indoor applications. To compensate for the lower power that LEDs generally emit, arrays of them can be used as optical sources. The penalty, however, is the bandwidth. Lasers can have speed into the gigabit-per-second regime, but LEDs are typically limited to 10 Mb/s, perhaps extending to 50Mb/s for some specialist devices [6]. Point-to-point designs minimize the transmitter power requirement and thus permit the use of a simple, low-cost receiver. Typically these links transmit using a single LED which emits an average power of several tens of mW, that is concentrated within a semi-angle of 15–30°, with emission wavelength typically lying between 850 and 950 nm. This

wavelength typically matches the responsively peak of the silicon P-Intrinsic-N (PIN) photodiodes.

2.2.3 OPTICAL DEMODULATOR AND RECEIVER

In the IM-DD channel, the input to the receiver cannot be negative [1,2,6]. The input signal to the infrared receiver represents power, which is then converted into photocurrent. That is, the total photocurrent y(t) produced by a photodetector is proportional to the integral of the squared electric field over the entire photodetector surface. The background light induces a high intensity shot noise in the photodetector compared to this shot noise, the electronic thermal noise in a well designed preamplifier will be negligible. In practice, there will be some restriction on average transmission power due to eye safety consideration. Modulation schemes that operate efficiently in the conventional channel may not necessarily be suited to IM-DD channels.

The two practical options for photodetectors in direct detection (DD) are PIN diodes and avalanche photodiodes (APD). PIN detectors are simpler devices with no internal gain. APDs with their internal gain are capable of detecting very weak signals which are weaker and generally it is possible to approach shot noise limited operation by careful receiver designs and careful choice of APD gain. In general, indoor systems use PIN photodiodes as they are cheaper, easy to bias and do not add any extra noise. The wavelength band near 800nm is attractive due to the availability of low cost high power GaAs laser diodes and large area silicon PIN diodes. This wavelength typically matches the responsivity peak of the silicon PIN photodiode.

The optical wireless receiver differs from their fiber optics counterparts in two significant ways. First, the dominant source of noise in fiber optic receivers either arise from the signal itself or the dark current in the detector. In an optical wireless receiver, the dominant source of shot noise in the detector arise from the ambient light levels in the environment, necessitating the use of optical filters in detectors. In fiber optic receivers the optical power is received as a concentrated beam permitting the use of extremely small detectors. By contrast, in an optical receiver, large area photodiodes are required to capture as much as signal possible. The large capacitance associated with such detectors, give rise to significant f^2 noise terms and preamplifier design methodologies must take this into

account if shot noise limit operation is to be achieved [6]. With the help variety of bootstrap receivers using PIN and APD of different dimension, a sensitivity ranging – 45dBm up to data rate 155 Mb/s is reported. But in most of the cases data rates above 100Mb/s have only been done demonstrated in laboratories [6]. Sensitivity improves as the photodiode area reduces because of the correspondingly lower capacitance. However, a smaller area photodiode incur a greater coupling loss due to the small aperture they present to the incoming beam, so a careful trade off between these factors is necessary to optimize the final performance.

2.3 IrDA STANDARD FOR INDOOR SYSTEMS

By 1993, several commercial products where available for point- to- point indoor optical systems. In order to provide effortless communication between various types and brands of equipments it was necessary to set standards for indoor IR communication. From this vision IrDA standards evolved. Now it is one of the most successful and widely adopted standard, which is based on a short-range 'point and shoot' philosophy. The IrDA (Infrared Data Association) was established in 1993 with the aim to create standards for interoperable, universal two way cordless infrared light transmission data port. IrDA technology is already incorporated in over 100 million electronic devices including desktop, notebook, palm PCs, printers, digital cameras, public phones/kiosks, cellular phones, pagers, PDAs, electronic books, electronic wallets, and other mobile devices. Depending on the data rates to date IrDA has split the physical layer into three distinct data ranges: 2400 to 115,200 bits/s (SIR Systems), 1.152 Mbits/s (MIR Systems) and 4 Mbits/s (FIR systems) and specified physical and protocol standards [6,7,8,9,23,24].

When IrDA was established, one of the major goals was to have a standard which is adaptable to a broad range of mobile appliances that needs connection to peripheral devices and host. IrDA chose the short-range, walk-up, point-and-shoot, directed infrared communications model for two reasons. First, it was perceived that the initial target market for IrDA-enabled devices would be mobile professional who is also a computer user. Second, IrDA chose this communication model to minimize cost. Using these

requirements, the IrDA committee developed a series of standards aimed at providing ubiquitous, low-cost, directed infrared communications for all classes [6,7,8,9,23,24].

2.3.1 IrDA ARCHITECTURE

The IrDA specifications provide guidelines for link access (IrLAP – Link Access Protocol), link management (IrLMP- Link Management Protocol) and for the electrical-optical hardware interface (Physical Layer) The protocol is arranged as a stack, where data from application programs are passed down through the stack and eventually transmitted as light pulses. An IrDA protocol stack is the layered set of protocols particularly aimed at point-to-point infrared communications and applications needed in that environment. The layers within the protocol stack can be divided into two groups – required and optional protocols. IrLAP, IrLMP and IAS (Information Access Service) are the three software layers of the protocol that are required in addition to the physical layer. The layer arrangements is as given in Fig. 2.4.

2.3.2 IrDA PHYSICAL LAYER

The IrDA physical layer is split into three distinct data rate ranges: 2400 to 115,200 bits/s (SIR Systems), 1.152 Mbits/s (MIR Systems) and 4 Mbits/s (FIR systems) and specified physical and protocol standards. Initial protocol negotiation takes place at 9600bits/s, making this data rate compulsory. Other data rates are optional. The links are designed to be used in a line-of–sight, point-and-shoot manner.

a). SHORT INFRARED (SIR) SYSTEMS

The baud rate of SIR systems is 2400 to 115,200 bits/s. Infrared receivers contain a high pass filter to remove background light. This high pass filter forces the use of encoding on the link to ensure that long strings of zeros and ones are not lost in transmission. The encoding used on this link is return-to –zero (RZ). Zeros are represented in this encoding scheme by a pulse of 3/16 bit duration and one by the absence of a pulse. This kind of coding is power efficient since infrared light is only transmitted for zeros. The tall narrow pulse has better signal-to-noise ratio performs than a short wide pulse of the systems. Data format is the same as for a serial port, i.e. asynchronously transmitted word, with a start bit

at the beginning. Transmitter can use either 3/16 mark-to-space ratio for one bit, or a fixed length 1.63μs of each optical pulse, which would correspond to 115kb/s. With fixed length and speed of 38400 b/s, each bit would take 3 pulses. The main disadvantage of SIR transceivers is that they are slow in coping with high data application, imaging applications and internet through wireless application protocol (WAP). The figure (Fig 2.3) gives details of SIR encoding scheme.

b). MEDIUM INFRARED (MIR) SYSTEMS

The baud rate of MIR systems is 1.152 Mbits/s. IrDA based MIR systems uses encoding of 1/4 mark-to-space ratio up to 1.152Mb/s and such systems use packet framing and CRC generation, and checking with the help of hardware. At these speeds, the basic unit (packet) is transmitted synchronously, with a starting sequence at the beginning. The details of encoding is given in Fig 2.5 .The NRZ signal in the figure is the original data signal without modulation.

c). FAST INFRARED (FIR) SYSTEMS

The data rate supported by FIR systems is 4 Mb/s. For 4Mb/s speed, the so-called 4PPM modulation with 1/4 mark-to-space ratio is used. Two bits are encoded in a pulse within one of the four possible positions in time. So, information is carried by the pulse position, instead of pulse existence as in previous modulations. A phase locked loop is used for recovering sampling clock from the received signal. Most of the commercial applications like digital cameras, scanners, toys and games use this mode. In 4PPM scheme two data bits are combined to form a 500ns data bit pair. This data bit pair (DBP) is divided into four 125ns time slots or chips The two bits to be encoded will have one of the four states 00, 01, 10 or 11. Depending upon which of these states is present, a single pulse is placed in either the first, second, third or fourth 125ns time slot. Thus a demodulator, after phase locking on the incoming bit stream can determine the data pattern by the location of the pulse within the 500ns period. IrDA recommended encoding details are given in Table 2.2.

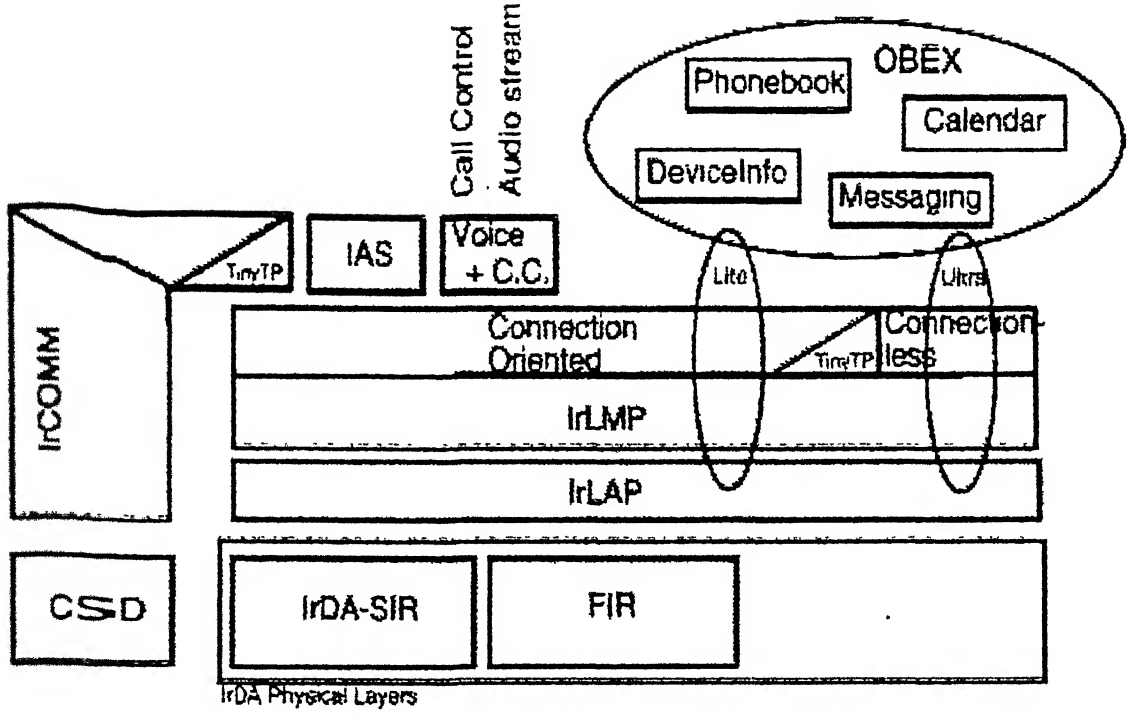


Fig 2.4 IrDA Architecture

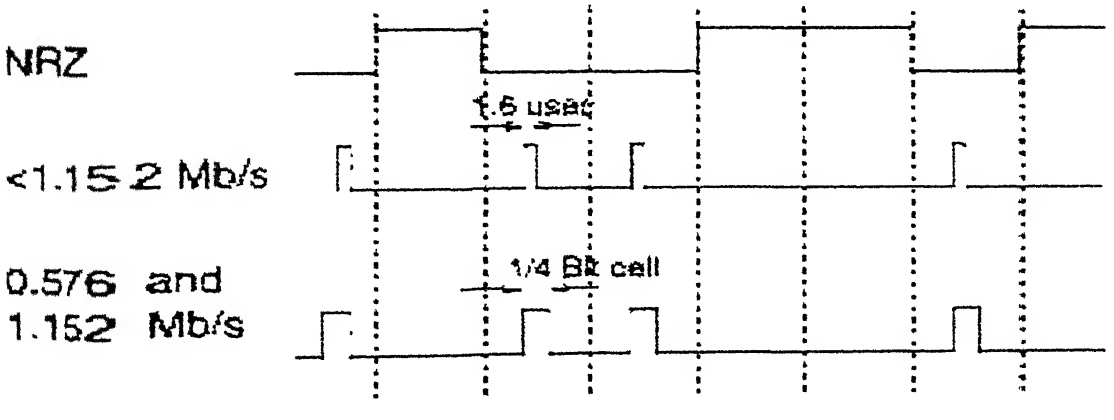


Fig. 2.5 Transmitted Signal for 0.576Mb/s &1.152Mb/s [7]

BIT PATTERN	PULSE POSITION
00	1000
01	0100
10	0010
11	0001

Table 2.2 PPM Encoding Scheme for FIR[7]

2.3.3 IrDA PROTOCOL LAYERS

a). IrLAP- LINK ACCESS PROTOCOL

The first layer above the physical layer is the Link Access Protocol (IrLAP). This layer is an IR adaptation of the HDLC (High Level Data Link Control) protocol. The function of this layer is to support link initialization, device discovery and conflict resolution, connection, startup, data exchange, disconnection, and link shutdown. IrLAP specifies the frame and byte structure of IR packets as well as the error detection methodology for IR communication.

b) IrLMP- LINK MANAGEMENT PROTOCOL

The link management protocol is layered on top of the IrLAP and has two main functions; application and service discovery and multiplexing of application level connections over the single IrLAP connections The IrLMP layer allows individual users to connect and exchange information with similar entities in the peer device, independent of any other service user using IrLAP connection. IrLMP's goal is to detect presence of devices offering a service, to check data flow, and to act as a multiplexer for configurations with more devices having different capabilities. Applications use the IrLMP layer to ask if a required device is within range etc.

c) IAS - THE INFORMATION ACCESS SERVICE

The IAS acts as the yellow pages for a device. All of the service/ applications available for the incoming connections must have entries in the IAS, which can be used to determine the service address. The IAS can also be queried for additional information about services A full IAS implementation consists of client and server components. The client is the component that makes inquiries about services on the other device using the information access protocol. The server is the component that knows how to respond to inquiries from an IAS client. The server uses an information base of objects supplied by local services and applications.

d). TINY TP - IrDA TRANSPORT PROTOCOLS

This layer manages virtual channels between devices, performs error corrections (lost packets, etc.), divides data into packets, and reassembles original data from packets. It is almost similar to TCP.

e). ROBE - IrDA OBJECT EXCHANGE PROTOCOL

This is a simple protocol, which defines PUT and GET commands, thus allowing binary data transfer between devices. It is built on top of Tiny TP. The standard defines what a packet must contain in order for the devices to recognize each other and communicate.

2.4. LIMITATIONS AND SAFETY ISSUES IN IR SYSTEMS

2.4.1 SAFETY ISSUES [6,5]

Eye skin safety and is one of the primary constraints in any optical wireless system. Although the eye can only see light between 400 nm and 700 nm, the eye is transparent to light with wavelengths well into the infrared beyond 1000 nm. If the eye looks towards powerful sources of invisible infrared light, this will focus down on the retina at the back of the eye, cause local heating to the tissue and possibly some permanent damage. All the optical sources used in indoor applications must conform to the Class-1 classification

(inherently safe) as per the IEC 825-1 standard. The eye safety limit is described by the accessible emission limit (AEL), which is a function of the viewing time, wavelength and size of the optical source. A distinction is drawn between point sources, which eye can focus and large extended sources, which form extended image on the retina. Currently IEC 825-1 makes no distinction between laser and LED. Laser light is far more dangerous to the eyes than LED light of the same power. This is because laser light can be focused on the retina to a very small spot, several wavelengths in diameter, where the light power intensity is correspondingly great. The only advantage of LED sources over lasers is that they are in general large and hence produce large angular subtends (α). So if viewed the image from the LED on the retina of the eye covers a larger area and hence the power is diffused. Even arrays of LEDs can produce substantial launch powers and yet be Class-1 eye safe. So indoor systems mostly use LEDs as emitters with powers less than 0.5mW. In order to overcome the strict power limitations that apply to point sources, several workers have used holograms so that a source operates in the extended source regime. Lasers operating inside the Class 3B band can infact be rendered Class 1 eye safe by passing it through a hologram. The hologram breaks up the wavefront in the optical beam, which diffuses the image of the laser spot on the retina of the eye. Even a 40 mW Class 3B laser can be made Class-1 eye safe, and with certain refinement in hologram 100 mW lasers can also be made safe. This technique is proven in laboratory but has yet to be taken up by the industry. The limiting constraint on transmitted power from such an extended source will be due to the power in the undiffracted beam from the diffuser. The classification for a point-source emitter is shown in Table 2.3. Table 2.4 shows Class 1 point source power limits. So in most of the cases indoor optical systems uses LEDs as there source for eye safety.

As per a Table 2.3, Class-1 eye safety limit for 850nm is approximately 0.5mW. From Table 2.4 it is clear that for 850nm the AEL is 0.44mW. Since LEDs come in this range it is preferred as optical sources, especially for indoor applications.

Classification	650 nm (Visible)	880 nm (IR)	1310 nm (IR)	1550 nm (IR)
Class 1	Up to 0.2 mW	Up to 0.5 mW	Up to 8.8 mW	Up to 10 mW
Class 2 *	0.2 – 1 mW	N/A	N/A	N/A
Class 3A	1 – 5 mW	0.5 – 2.5 mW	8.8 –45 mW	10 – 50 mW
Class 3B	5 – 500 mW	2.5 –500 mW	45- 500 mW	50 –500mW

* Class 2 applies only to visible light sources.

Table 2.3 Laser Safety Classification For a Point- Source Emitter [5].

Wavelength	Point Source AEL $\alpha < \alpha_{min.}$	Extended Source AEL $\alpha_{min.} < \alpha < \alpha_{max}$	Extended Sources AEL $\alpha > \alpha_{max}$
850 nm	0.44 mW	0.44 (α/α_{min}) mW	0.8 ($\alpha_{max}/\alpha_{min.}$) mW
980 nm	0.8 mW	0.8 ($\alpha/\alpha_{min.}$) mW	0.8 ($\alpha_{max}/\alpha_{min.}$) mW
1300 nm	8.8 mW	8.8 (α/α_{min}) mW	8.8 ($\alpha_{max}/\alpha_{min.}$) mW
1500 nm	10 mW	10 ($\alpha/\alpha_{min.}$) mW	10 mW

Notes:

1. For exposure times greater than 1s. $\alpha_{min} = 0.011$ and $\alpha_{max.} = 0.1$ rad.
2. AEL is equal to power captured by 50 mm diameter aperture 100 mm from the optical antenna. In most cases AEL is equal to the emitted power.

Table 2.4. Class 1 Point Source Power Limits [6].

2.4.2 INTERFERENCE FROM AMBIENT LIGHT [5,6,27]

In an optical wireless receiver, the dominant source of shot noise in the detector arises from the ambient light levels in the environment. Because of wide field of view (i.e. aperture) of a free space optical receiver, stray light in addition to wanted light could reach the photodiode. Ambient light raises the level of photonic noise in the receiver and hence can impair performance. The main three sources of ambient light sources are sunlight, fluorescent light and tungsten lamps. The normalized power spectral densities (PSDs) of sunlight peak at around 500nm and have still have relatively high spectral weighting at 1100nm(the approximate cut-off wavelength of silicon), while the PSD of fluorescent light peaks at approximately 600 nm and extents into near infrared region Tungsten lamps have extremely broadband spectra, peaking at around 1000nm. The properties of ambient light sources lend themselves to straightforward remedies. First by placing a narrowband infrared filter over the photodiode, the level of ambient light relative to the wanted beam will be significantly reduced. Infrared filters may be fabricated in glass or plastic, depending on the optical quality required and application. It can seen that with a 50 nm optical bandwidth, the ambient photocurrent varies over four orders of magnitude depending on environmental conditions. The optical environment is progressively quieter with increasing wavelength, thus it is found attractive to work in 1400nm level. But the systems to date have concentrated on the 800-900 nm region where low cost silicon technology can be employed. GaAs based devices are also available at present The power spectral density of ambient induced noise extends from DC to typically a few tens of kilohertz, exceptionally a few hundreds of kilohertz, depending on the type of the source. By conveying the data over the optical beam on a high frequency sub-carrier, or more commonly by applying a line code that contains no low frequency components, interference is entirely avoided. The strong DC content due to ambient light can cancel by optical filters and a receiver design that blocks any DC from the photodiode.

2.4.3 ATMOSPHERIC LOSS [5,6,27]

The power budget and overall performance of a point-to-point free space link is strongly determined by atmospheric loss along the propagation path. The various atmospheric losses are free space loss, clear air absorption, scattering, refraction and

scintillation. Out of all these types, only free space loss affects the performance of point-to-point indoor systems. Free space loss is defined as the proportion of optical power arriving at the receiver that is usefully captured within receiver aperture. A typical figure for a point-to-point system that operates with a slightly diverging beam would be 20 dB, whereas an outdoor system can have a free space loss of 40dB or more.

2.4.4 SPEED OF TRANSMISSION

Most commercial LEDs cannot be operated at speeds greater than 155 Mb/s. At this time, optical wireless systems requiring greater payloads such as 622 Mb/s and above must use laser sources. However, most of them are not useful for indoor optical communication due to the eye safety issue.

2.5 RECENT DEVELOPMENTS AND FUTURE OF INDOOR IR LINKS

As portable computers and communication terminals become more powerful and more widely deployed, the demand for high-speed wireless link is increasing. So IR represents an alternate choice for many short-range applications due to its wide bandwidth, simple circuits and economical viability. Despite problems such as, shot noise due to ambient light, limitation in bandwidth due to the capacitance of large area photodiodes, multipath propagation, many commercial devices are presently available for various optical wireless transmission. The various point-to-point IR applications in the market are in the field of computing segment, telecom, consumer electronics and peripherals. IrDA compliant trans-receivers are available to operate at up to 4Mb/s. IrDA is in the process of bringing out standards for very fast infrared (VFIR) at a data rate 16Mb/s. Those products based on VFIR will push the cost versus performance curve to a new level bringing end users faster throughput without substantial increase in the cost. The VFIR links will be fully compatible with FIR and SIR links. VFIR addresses the emerging user demand for digital cameras, scanners, portable storage devices and IR LAN access points for notebooks as well as desktop PCs [29]. Other commercially available systems operate at 10 Mb/s over a span of 10m. Experimental systems have been used to demonstrate cellular networks

operating at 155 Mb/s up to 4 km and also up to 1 Gb/s over 40 m (in outdoor IR links). In diffuse indoor optical systems experimental results have been satisfactory up to 25 Mb/s in a room of 10 m on each side, although higher rates have been demonstrated under particular conditions [5]. The Infrared data association has projected a total shipment of 1.3 billion units by the year 2003. This high IR adoption rate reflects the presence of more IR applications in the marketplace than ever before, with penetration rate for some segments reaching 100% [29].

CHAPTER 3
DESIGN OF FIR INDOOR POINT- TO- POINT LINKS

The major aim of this thesis is to design and develop an IrDA compatible indoor point-to-point FIR experimental link. This chapter gives the design details and system considerations for the implementation such a link. The subsystems to be designed are the transmitter and receiver. The transmitter consists of a 4PPM encoder, FIR packet framer and source-driver electronics while the receiver has a sensitive optical receiver, bit synchronizer and a 4PPM decoder. The design specifications are:

- Modulation - 4PPM
- Bit error rate - less than 10^{-9}
- Directionality - Line of sight
- Range - 10 cm, typical

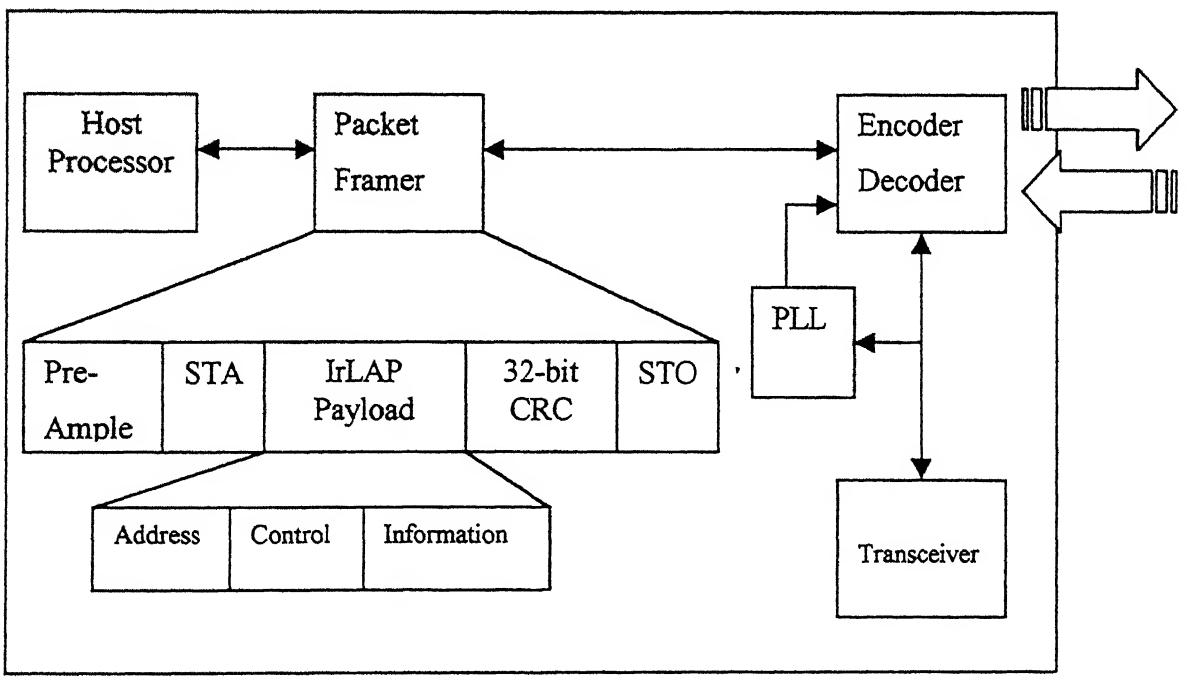


Fig 3.1: Block diagram of FIR infrared communications transceiver. This is used for high-speed communications at 4Mb/s. Due to the more stringent requirements for clock timing, a digital phase-locked loop (PLL above) is

3.1 CHOICE OF SUB- SYSTEM ELEMENTS FOR TRANSCEIVER

The essential subsystems of an indoor point-to-point IR links are the optical transmitter and receiver. In design of these subsystems the choice of a suitable source and a detector depends on cost, size, and wavelength of operation and power consumption and also on the maximum safety levels without degrading the performance of the system. The receiver front end also needs to be chosen based on bandwidth, sensitivity etc.

3.1.1 CHOICE OF THE OPTICAL SOURCE

The optical source is a major component in any optical communication system. Its fundamental function is to convert electrical energy in the form of a current into optical energy, which effectively transmit light energy to the receiver. The two major considerations for the source selection in indoor point-to-point IR links are, the power requirements and the personal eye safety. Two types of semiconductor sources that are available for indoor links are LEDs and Class-1 eye safe laser diodes (LDs). LEDs show linear behavior in their optical power vs. current characteristics. Also, LEDs are rugged and have high life time. Low cost laser diodes are attractive, especially for outdoor applications. However, for indoor applications laser poses a potential safety hazard because they are point source emitters. LEDs, on the other hand, are large area emitters and thus can be operated safely at relatively higher powers [1,2]. They are therefore the preferred emitter for most indoor applications. Typical packaged LEDs emit light into semi-angle (at half power) ranging from about 20^0 to 40^0, making them suitable for directed indoor transmitters.

The wavelength of operation is another important design consideration. Due to rapid developments in fiber optic systems LED and laser diode optical sources are available at 850nm, 1300nm and 1550nm. AlGaAs or GaAs sources emitting light in the ranges of 820nm - 900nm are the ideal sources for most applications of indoor infrared wireless links from the point of view of cost and available power output. To compensate for the lower power that LEDs generally emit, arrays of them can be used as optical sources. The penalty, however, is bandwidth. Lasers can have speed into the gigabit-per-second regime; LEDs are typically limited to 10 Mb/s, perhaps extending to 50Mb/s for some specialist devices. Point-to-point designs minimize the transmitter power requirement and permit the use of a simple, low-cost receiver. So typically these links, transmit using a single LED that emits an average power of several tens

of mW that is concentrated within a semi-angle of 15° –30°, with emission wavelength typically lying between 850 and 950nm. This wavelength matches the responsivity peak of the silicon PIN photodiode.

Compared to the LDs, LEDs can offer the advantages of higher reliability, reduced temperature sensitivity, less complicated drive circuit requirements, immunity to optical feedback and lower cost due to high yields and packing technology. Taking all these factors into consideration, in our design an LED source with a wavelength 850nm was chosen.

3.1.2 CHOICE OF OPTICAL DETECTOR

The photodetector is an opto-electronic device that absorbs optical energy and converts it into electrical energy, which is amplified and processed to deliver information in a useful format. The performance requirements of a detector are high sensitivity, low noise, wide bandwidth, high reliability and low cost. For communication applications, there is usually a need for high-speed detectors. For several other applications high gain is required. Therefore, bandwidth and gain are fundamental physical trade off parameters which decides, which photodetector is most suitable for a typical applications. But in optical wireless communication, the choice of photodetector depends mainly on three factors, viz. the response time, sensitivity of the receiver and noise due to ambient light. Two types of detectors have been generally used, PIN photodiodes and Avalanche photodiodes (APDs).

The upper limit of the response time is determined by the accuracy required or the demodulation bandwidth of the receiver signal. The two factors that limit the speed of response are the width of the depletion region and the magnitude of the electric field within that region ($t_{rise} = \frac{W}{v_{max}}$ where W is the width of the depletion layer and v_{max} is the drift velocity). Since external load resistance of the photodetector also affects response time through the chip capacitance, which should be reduced for a good receiver. A small detector area provides low dark current and minimizes capacitance allowing larger load resistance for a given response time. The response time of 1-100ns is generally required.

The quantum efficiency of a photiodetector (η) is defined as the ratio of the number of electrons collected to the number of incident photons. One of the major factors, which determine the quantum efficiency, is the absorption coefficient of the semiconductor material used in photodetector. The expression for quantum efficiency does not involve photon energy and

therefore the responsivity R is often used for characterizing the performance of photodetector. It is defined as $R=\frac{I_p}{P_o}$ (A/W) [1] where I_p is the photocurrent and P_o is the incident optical power

A responsivity of 0.5 A/W - 0.6 A/W is generally required. The GaAs PIN diodes can provide high quantum efficiency and bandwidth. However, the bandwidth of commercially available GaAs packaged detectors is limited to 1 to 2 GHz due to the limitations in packing.

The choice between the APD and PIN photo diode will often be made on the basis of the cost versus sensitivity. Sensitivity is more for APD but noise due to dark current is also high. Some of the important factors, which lead to the selection of PIN diode for this application, are given below.

- Even though APD provides higher sensitivity than PIN diode, the dark current is also higher. In digital receivers this higher noise in the "no optical signal present" condition will increase the probability of error.
- Since APD gain is a strong function of this voltage, it requires high voltage power supplies with very good regulation.
- PIN photo detectors are 20 times less expensive than APD.
- The additional noise produced by the ambient light focused on to the device cancels much of the gain advantages of the APD over PIN.

Hence the ideal choice for optical receiver for indoor applications is a PIN photodetector.

3.1.3 CHOICE OF THE RECEIVER FRONT-END

The current generated by a photodetector is converted into a useful signal by the front-end preamplifier. The signal from preamplifier is further amplified by post amplifier and then connected to a high speed comparator to convert it into digital form. Two commonly used front-end configurations for pre-amplifiers are the high impedance (HZ) type and the transimpedance (TZ) type. In the high impedance type all sources of noise are minimized since noise current is inversely proportional to the impedance. Its main advantage is that it has sensitivity higher than the TZ type. However, its dynamic range is limited and equalization of pulses is necessary. TZ type provides a wide bandwidth and greater dynamic range although the noise performance is inferior to HZ type. TZ type front end was preferred due to the simplicity of practical realization and its greater dynamic range and bandwidth.

A transimpedance amplifier is shown in Fig.3.2. This configuration largely overcomes the drawbacks of the high impedance amplifier with negative feedback This device therefore operates as a current mode amplifier where the high input impedance is reduced by the negative feedback A low output noise level requires the use of a high value R_F and a low value C_T. The amplifier however has a pole at an angular frequency of $\frac{G}{R_F C_T}$ [26], so as R_F increases the bandwidth of the circuit would be reduced necessitating more equalization. To overcome this the open loop gain G may be made as large as the stability of the closed loop would allow The closed loop voltage transfer function of the TZ configuration shown in Fig.3.3 is given by [1]

$$H_{CL(\omega)} = \frac{R_F}{1+(j\omega R_F C_T / G)} \ (\mathrm{V\,A^{-1}}).$$

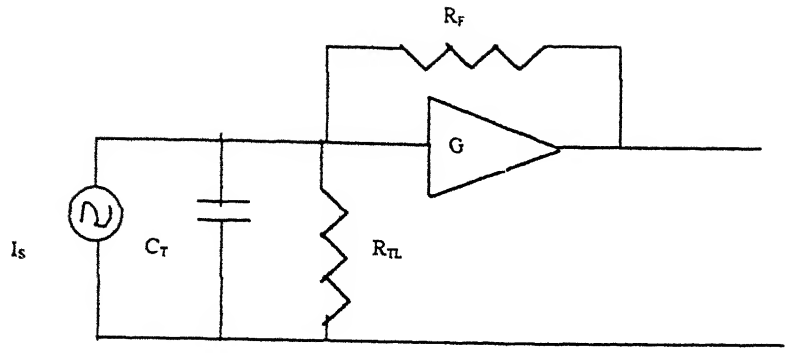
Here the electric bandwidth B_1 (without equalization) is

$$B_1 \leq \frac{G}{2\Pi R_F C_T}$$

The bandwidth of the amplifier without negative feedback is

$$B_2 \leq \frac{1}{2\Pi R_{TL} C_T}$$

The design of the first stage of the preamplifier requires particular attention, since most of the amplifier noise is contributed by this stage. The first stage may be implemented using either a FET or BJT. In the frequency range of our interest (below 10 MHz) commercially available. JFETs are less noisy than commercially available bipolar transistors. Hence JFET was chosen as the active device for the first stage. The first stage FET is operated optionally in common source mode. In this mode the input impedance, output impedance and power gain are high, and hence it minimizes the noise contribution to the subsequent stages. In order to have low amplifier input capacitance C_a, the voltage gain of the FET should be reduced. This can be achieved by following the common source stage with a stage having low input impedance BJT is chosen as the second active device to ensure good bandwidth Shunt feedback stage following the FET was preferred as it offers better rejection of the noise from the succeeding stages without introducing noise itself. Another advantage of the shunt feedback stage is its low output impedance, which reduces the effect of loading from the next stage.



$$R_{TL}=\frac{R_a R_b}{R_a + R_b}$$

R_a= amp i/p resistance
R_b= bias resistor
C_T= C_d+C_a
C_d= diode capacitance
C_a= amp i/p capacitance.

Fig:3.2 Transimpedance Pre-Amplifier [26]

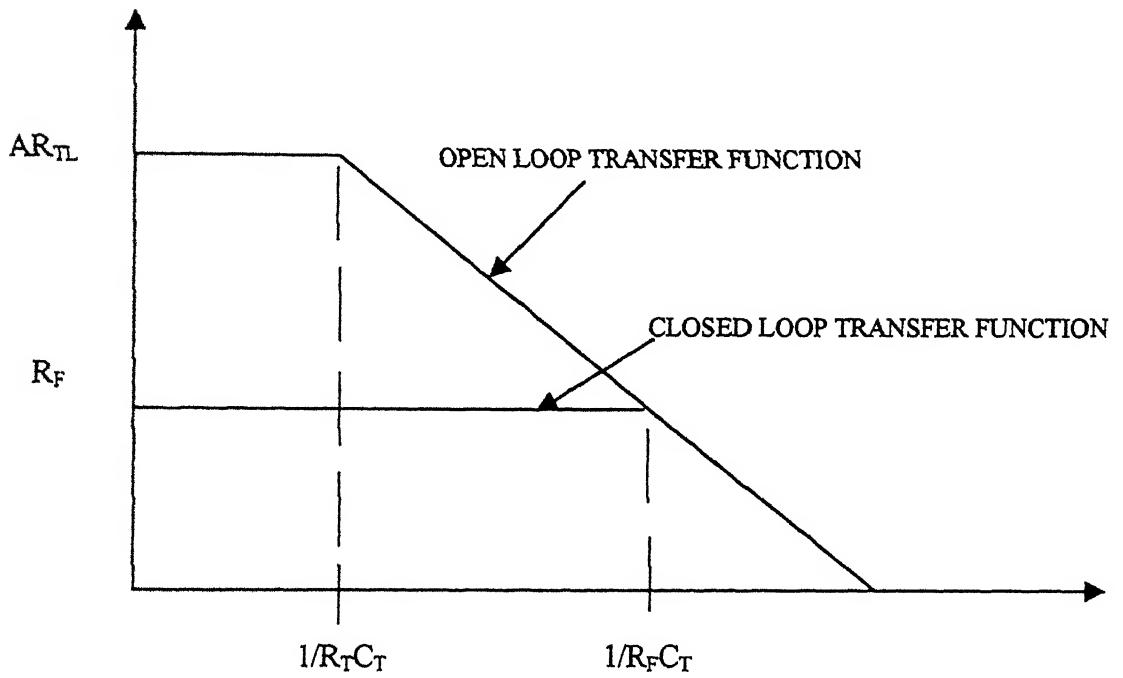


Fig.3.3 TZ Amp. Transfer Function [26]

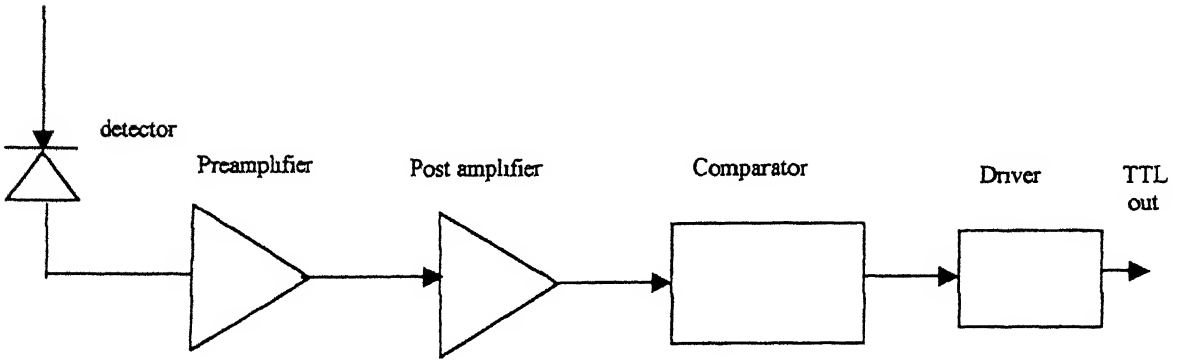


Fig 3.4 Schematic of an optical receiver

The schematic of an optical receiver is as shown in Fig. 3.4. The preamplifier circuit was designed for a sensitivity of –40dBm at 10 Mb/s, and is followed by a post amplifier, which is implemented by a differential video amplifier The output of the postamplifier is given to a hard limiter designed using a high speed comparator followed by and a TTL compatible line driver circuit.

3.2 DESIGN OF AN IrDA COMPATIBLE FIR PACKET FRAMER

IrDA compatible FIR packet framer consists of a 4PPM encoder and a packet wrapper. The wrapper type used for 4 Mb/s is synchronous 4PPM framing. The wrapped data is given to the input of the optical driver circuit to transmit it through LED source. The 4Mb/s physical layer packet has distinct features that perform a useful and well-defined role. The details of the 4PPM encoder and packet wrapper are discussed below.

3.2.1 4PPM ENCODER

Pulse position modulation is used as the line code for the 4 Mb/s FIR link. Data is transmitted within a PPM signal by varying the position of a pulse (referred to here as chip) within a symbol (referred to here as cell). The PPM modulation for the 4 Mb/s link allows one chip to be set in one of the four possible positions, and hence the name 4PPM. Since a chip can be set in one of the four possible positions, four different messages can be sent within one cell, allowing two bits of data to be encoded per cell. Fig. 3.5 shows the four possible messages that can be transmitted by 4PPM. Properties and advantages of 4PPM were detailed in Chapter 2. To create a 4PPM encoded output from data as shown in Fig. 3.5, we used the following approach as shown in Fig.3. 4. IrDA standards do not specify any particular implementation scheme for the physical layer and is left to the hardware designer's choice. The block schematic of Fig.3.4 was designed in our work with simple discrete components. Here for generating serial test data a PRBS (pseudo random bit sequence) generator with a data rate of 4Mb/s is used.

The encoder takes the data serially. The input data is first converted from serial bit stream to parallel data in groups of two bits each, which is then loaded into the select inputs of the 4-to-1 multiplexer. Simultaneously to create chips at a frequency of 8MHz, a two bit synchronous counter with a clock frequency of 8MHz is used. From the two-bit output of the counter, all the four different cells for 4PPM are created with the help of a 2-to-4 decoder. These four decoded signals are provided as the inputs to a 4-to-1 mutiplexer.

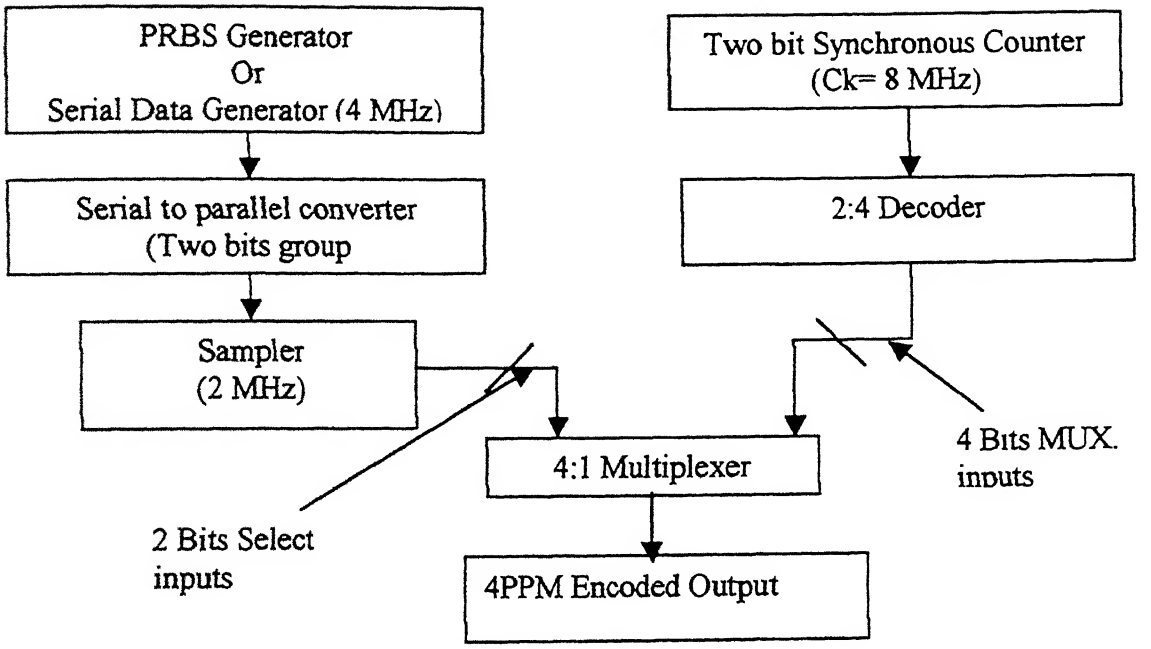


Fig.3.5 Block Diagram of 4PPM Encoder for FIR Transmitter

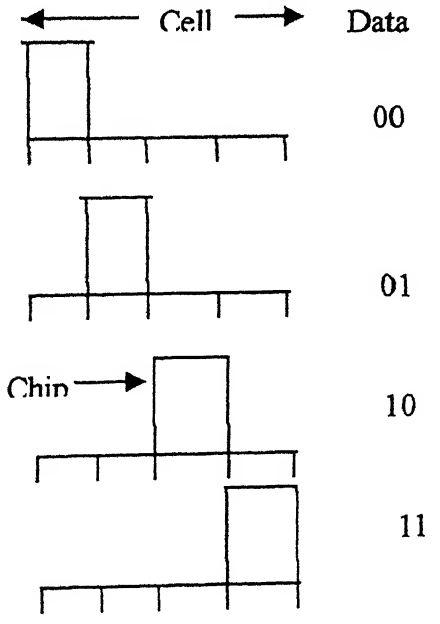


Fig. 3.6 4PPM Message Encoding [24]

One of these inputs will be sent out depending on the status of select input at a rate of 2MHz. Since the select input is varying at the frequency of 2MHz and counter output at the frequency of 8MHz, two bits of data is properly encoded into the required 4PPM mode.

3.2.2 DESIGN OF FIR DATA WRAPPER

The function of the FIR data wrapper is to wrap the preamble chips (PA), beginning of the frame chips, 4PPM encoded data and end of the frame chips (STO) into the form of a packet as per FIR standards, so that it can be directly provided to the driver of the optical transmitter. The format specified for the FIR packet shown in Fig. 3.6 [24].

Preamble 64 chips 8MHz	Start pulse 32 chips 8MHz	Serial data (2<n<2048) 4 MHz to be encoded by	CRC (32 bits) to be encoded by 4PPM	Stop Pulse 32 chips 8MHz

Fig. 3.7 Format of A FIR Packet

A preamble (PA) allows dc balance to be attained, and also permits the phase-locked loop at the receiver to achieve chip-level synchronization. The start (STA) and stop (STO) delimiters provide cell and frame synchronization, and are chosen so as not to compromise the overall packet robustness or adversely affect the receiver eye diagram. To distinguish from PA and end limiters from the frame body, these fields contain code violations. The body of the packet is 4PPM- coded and has 32 bits cyclic redundancy check (CRC) field appended to it. It provides a guaranteed level of robustness to undetected data errors. The details of the PA, STA and STO are as given in the Fig.3.7, Fig.3.8 and Fig.3.9. The packet framing and CRC generation and checking are performed in hardware to relieve the burden on the host processor, while higher-level protocols are implemented in software on the host processor. In this thesis, CRC generation is not implemented due lack of time. The packet framer, ENDEC, and phase-locked loop are more complex than the UART and ENDEC used in the 2400 -115,200 bit/s links. However, this added complexity need not use expensive components as these hardware components can be added quickly and inexpensively to one of the host system's ASICs. PC chipsets including the 4 Mb/s hardware are already available from leading semiconductor manufacturers. No standard method has been defined for the implementation of IrDA physical layer and hence the hardware

designer can appropriately design the packet framer In our study, the hardware for generating PA, STA, STO, encoded data and packet framer were designed implemented by commonly available ICs and discrete components.

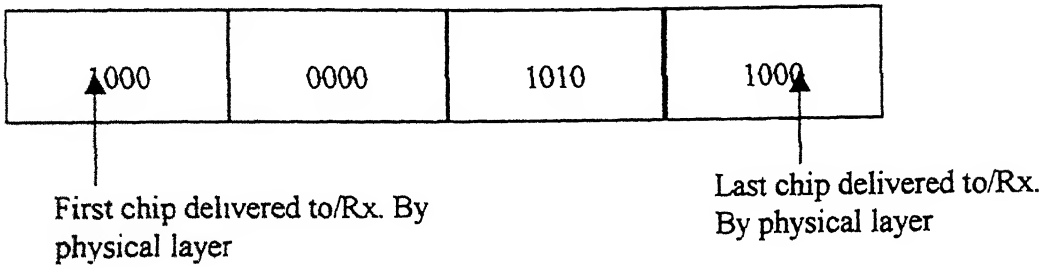


Fig. 3.8 Preamble Pattern [7]

0000	1100	0000	1100	0110	0000	0110	0000

Fig. 3.9 Start Pulse Pattern [7]

0000	1100	0000	1100	0000	0110	0000	0110

Fig.3.10 Stop Pulse Pattern [7]

Preamble 64 chips (8MHz)	Start Pulse 32 Chips (8MHz)	Serial Data (64 bits) (4MHz) (To be encoded by 4PPM) (64*2)= 128 chips	Stop Pulse 32 chips (8MHz)

Fig. 3.11 FIR Packet Wrapper for 64 Bits of Data with 4MHz Speed

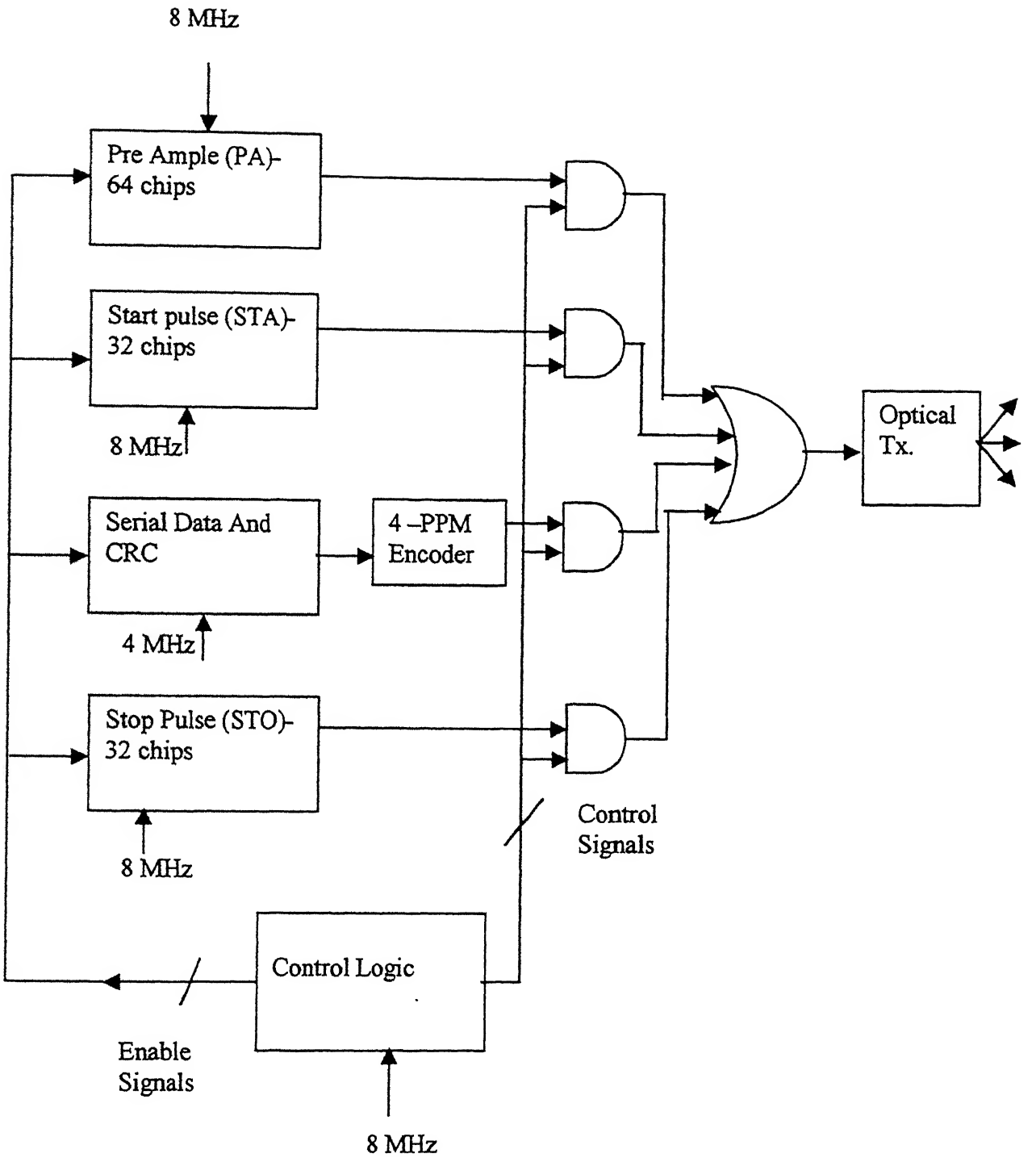


Fig.3.12 Block Diagram for FIR Data Wrapper and Transmitter

3.3 DESIGN OF IrDA COMPATIBLE FIR DECODER

IrDA compatible FIR decoder consists of a bit synchronizer for clock recovery, and a 4PPM decoder. A phase-locked loop replaces edge detection in SIR (short infrared) as the means of recovering the sampling clock from the received signal.

3.3.1 4PPM DECODER

The decoder receives the data serially which has an incoming data rate of 8 Mb/s. The block schematic of the decoder is shown in Fig. 3.13. The serial input data is converted into blocks of 4 bits and these 4 bits are provided to the input of 4:2 decoder, which converts it

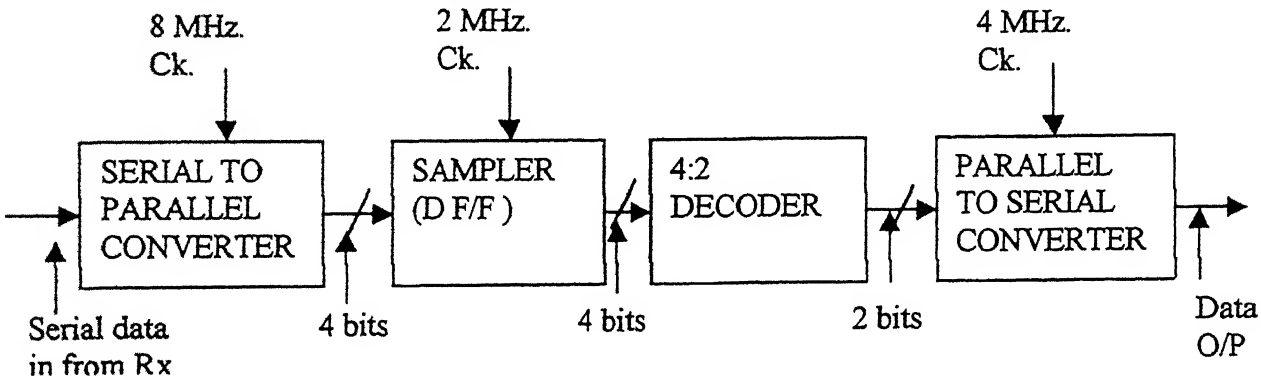


Fig. 3.13 Block Diagram of the 4PPM Decoder

DATA (AB)	ENCODED BITS $Y_3Y_2Y_1Y_0$
00	1000
01	0100
10	0010
11	0001

Fig:3.14 Truth Table for 4PPM Encoding

into two bits Let A and B are the MSB and LSB of the decoded output and $Y_3Y_2Y_1Y_0$ are the inputs as given in Fig.3.14 then

$$A = Y_0+Y_1$$
$$B = Y_0+Y_2$$

The 4:2 decoder is designed to work on this logic. This two-bit output of the 4:2 decoder is loaded into the parallel-to-serial converter and serial data is taken out at the rate of 4 MHz.

3.3.2 BIT SYNCHRONIZER

The UART-style clock recovery used in SIR (Short Infrared), utilizes a single signal edge to set the phase of the recovered sampling clock. This inevitably gives rise to phase jitter on the recovered clock and consequent signal to noise ratio penalty. The phase-locked loop used by the 4 Mb/s link generates a sampling clock with much less jitter because it uses timing information from many signal edges to set the phase of the clock.

The block schematic of a phase locked loop is shown in Fig. 3. 15. An analog phase locked loop could have been used for clock recovery and might have achieved a low phase jitter, but it would have been unable to achieve the rapid phase lock of a digital phase locked loop. Rapid phase lock is important in a packetized data system, because it determines the length of the training sequence, or preamble, required at the start of every packet to allow the phase locked loop to lock. The lock time is dictated by the accuracy with which the nominal frequency of the phase locked loop can be set. The nominal frequency of the variable oscillator in an analog phase locked loop is highly variable, since it is determined by the poor tolerance of the resistors and capacitors. By contrast, the nominal frequency of the variable oscillators in a digital phase locked loop can be locked to a crystal reference with a tolerance of less than 100ppm.

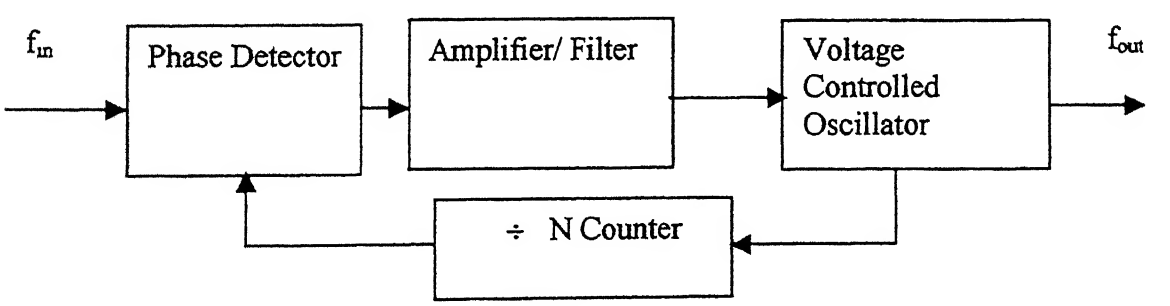


Fig. 3.16. Schematic of a Digital Phase Locked Loop

In this basic block diagram, the output frequency will be identical to the input frequency A fundamental loop consists of a phase detector, amplifier/filter and VCO. It appears and acts like unity gain feedback loop. The controlled variable is phase; any error between f_{in} and f_{out} is amplified and applied to the VCO in the corrective direction. In a digital phase locked loop the phase detector is a state machine that compares the edges in the received signal with those of the recovery clock (Rx_clock). The digital PLL circuit was designed and implemented with the help of a Motorola MC4044 Phase detector and a MC4024 VCO. Rising edges occur only in Rx. signal at PPM chip boundaries. Rising edges of Rx. clock should occur halfway between chip cell boundaries. If Rx. signal is earlier than expected, then the phase detector produces a Down signal, thereby advancing the phase of Rx clock If Rx. signal is later than expected, then the phase detector produces an Up signal. The average value of the resulting waveform is proportional to the phase difference between the two inputs. In a closed loop application, the error signal for controlling the VCO is derived by translating and filtering these waveforms. The VCO is designed so that its output frequency range is equal to or greater than the required output frequency range of the system. The free running frequency of the VCO can be varied by changing the value of the capacitance. The ratio of change in output frequency to the input control voltage is called gain constant. System dynamics when in lock are determined by the amplifier/ filter block. Its gain determines how much phase error exists between f_{in} and f_{out}

CHAPTER 4
IMPLEMENTATION OF INDOOR FIR LINKS

This chapter gives the implementation details of the FIR experimental link with discrete components. For the indoor systems the only permissible source is the LED. In this study, a single LED was used in the optical transmitter. The 4PPM encoded data, packetized with a proper preamble, STA and STO was transmitted through this optical transmitter. At the receiving end it was received by a PIN diode and the signal was recovered back with the help of a FET front end pre-amplifier. The clock from the received signal was recovered back with the help of a digital PLL. Implementation details of these various subsystems are explained in the following sections. Measured results are also provided.

4.1 FIR TRANSMITTER

FIR transmitter consists of a 4PPM encoder, preamble, STA and STO pattern generator, FIR data wrapper and optical transmitter. Test data was generated with the help of a PRBS generator and it was properly encoded with the help of 4PPM encoder and packetized with preamble, STA and STO bits and was then transmitted through an LED transmitter. The implementation details of each are discussed below.

4.1.1 4PPM ENCODER

The function of the 4PPM encoder is to encode the data generated by a PRBS generator at 4 MHz rate. Here in this experimental link, a packet of 256 chips was implemented. The details are shown in Fig 3.11. Out of those 256 chips, 128 chips were contained the 4PPM encoded data. With the help of a data wrapper these 128 chips of encoded data were transmitted from the 97^{th}clock to the 224^{th} clock (i.e. 61H to E0H). For generating these 128 chips of 4PPM encoded data at 8 MHz, 64 bits of data is required at a data rate of 4Mb/s. The details of the 4PPM encoder are given in Fig.4.1.

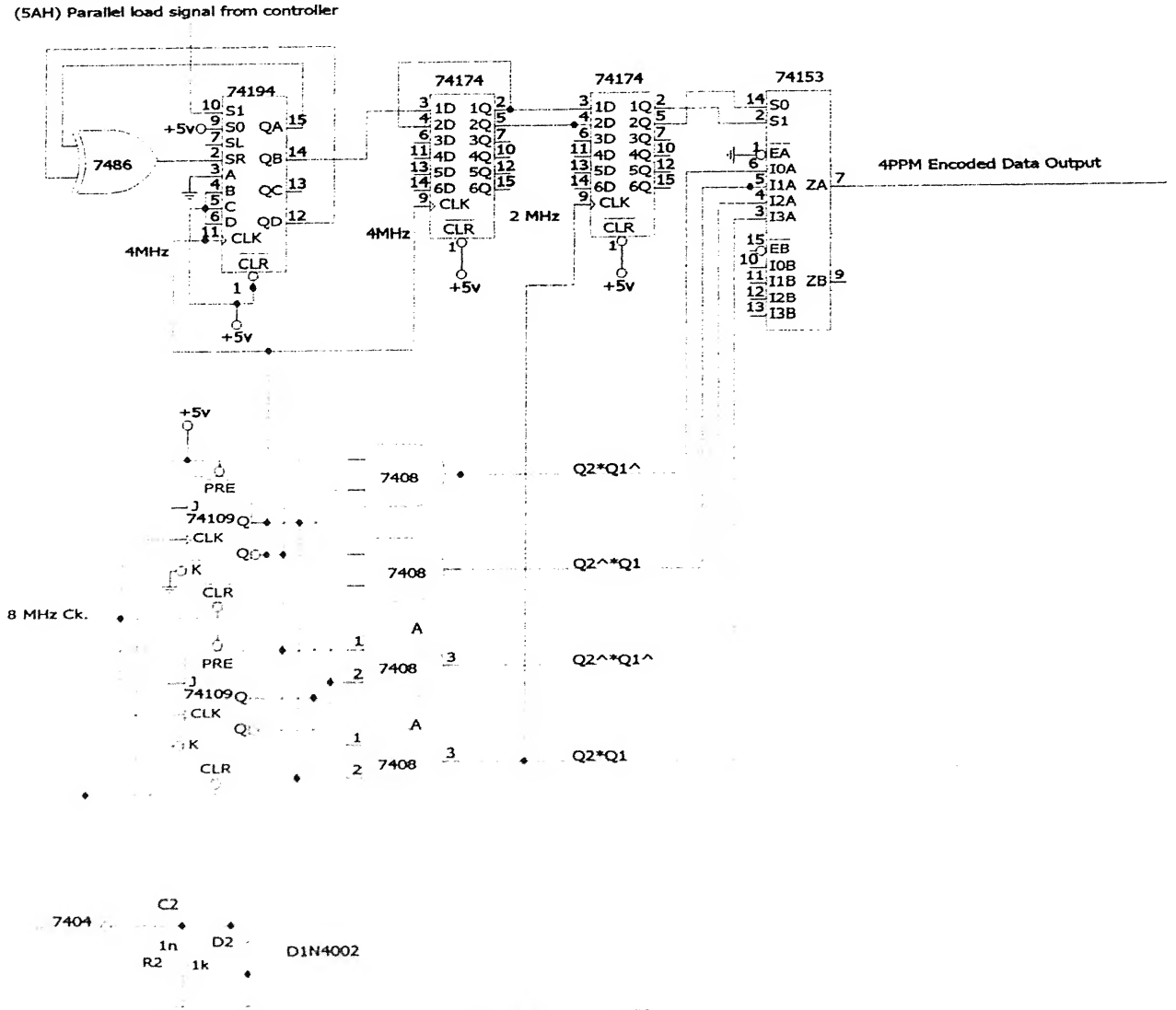


Fig.4.1. 4PPM ENCODER

a) PRBS GENERATOR

The serial data was generated with the help of a PRBS (Pseudo Random Bit Sequence) generator implemented with the help of a 74LS194 universal shift register and a 7486 EX-OR gates. The 74LS194 is a universal synchronous shift register with various modes like right shift, left shift, parallel load and hold mode. The encoder requires six clock signals for encoding data in 4PPM mode. At the optical transmitter, the data should be ready by the $61H^{th}$ clock. Hence a parallel load signal was derived from the $5AH^{th}$ clock from the master clock generator of the controller. The parallel load signal from the controller derived from the count 5AH loads a pattern of 1110 for the clock number 5BH to 74LS194. Then from next clock onwards it will work in the mode of serial in right shift, serial out mode. It is important to prevent the all zero state in a PRBS generator. The serial in data were derived from the output of the 74LS194 with the help of a X-OR and fed back to DSR (Data Shift Right) pin of the shift register The shift register was provided with a clock of 4MHz derived from a divide by two synchronous counter. This synchronous counter was controlled by the main controller. This PRBS generator generates the 15-bit repetitive pattern 111010110010001.

The serial data from this PRBS data generator is then divided into a group of two bits so as to be loaded into the select input of the 4:1 multiplexer for generating 4PPM encoded data. This is implemented with help of D- latches. Initially the serial output from the PRBS generator is provided to the input of a two bit serial in parallel out shift register implemented by 74LS174 D-latch clocked at a frequency of 4MHz. The output of this shift register is sampled at a frequency of 2MHz with the help of a parallel in parallel out shift register implemented by 74LS174 D-latch. For the synchronization purpose this 2MHz signal is derived from (Q_1.Q), obtained from the two bit synchronous counter output. These two bit outputs of the shift register at 2MHz are given to the select input of the 4:1 multiplexer implemented by 74LS153.

A 4:1 multiplexer was used for encoding the two bit data into a cell of 4 chips as shown in Fig.3. 6. The inputs of the multiplexer were generated with the help of a two bit synchronous counter and a 2:4 decoder. This two bit synchronous counter was implemented with the help of 74LS109 positive edge triggered JK flip flop clocked at

frequency of 8MHz Both flip-flops were reset with the help of a signal derived from the count 5AH from master counter so as to achieve proper synchronization in operation.

From the clock number 5BH onwards the counter starts to count up. The two-bit output of the counter was separated into 4 cells, with the help of a 2:4 decoder implemented by AND gates (74LS08). The four outputs of the 2:4 decoder were provided as the inputs of the 4:1 multiplexer. Since counter is working at frequency of 8 MHz, all the four cell combinations at a rate of 2MHz are present in the input of multiplexer as shown in Fig. 3.6. Depending on the select input status anyone of this cell was transmitted out from the 4:1 multiplexer. These encoded data bits were provided as the input to the optical transmitter.

4.1.2 PREAMBLE, STA AND STO PATERN GENERATORS

For packetizing data as per IrDA specification for FIR transmission, 64 chips of preamble, 32 chips STA (beginning of frame or start pattern) and 32 chips of STO (end of frame chips or stop pattern) are to be generated. The detailed circuit implemented for generating these patterns are as given in Fig. 4.2.

a) PREAMBLE

The preamble consists of exactly sixteen repeated transmission of the following stream of symbols at 8 MHz. In a PA field, the transmission time increases from left to right so that chips and symbols on the left are transmitted first. The sixteen bit pattern was 1000 0000 1010 1000 [7]. This was implemented with the help of four universal shift registers 74LS194. In the transmitting packet of 256 chips, the first 64 chips are the preamble patterns, i.e. from clock number 1 to 64 (01H to 40H). Parallel load control signal was derived from the clock 00H and with this signal the above pattern was loaded parallelly. From next clock onwards these four shift registers work in the right shift, serial out mode. Simultaneously the shifted out bit from the last flip-flop was loaded back to the DSR input of the first shift register. 64 chips of the PA were generated by four repeated transmission of 16 chips as above.

b) START FLAG

The start flag (STA) consists of exactly one transmission of the following stream of symbols. In the STA field, the transmission time increases from left to right

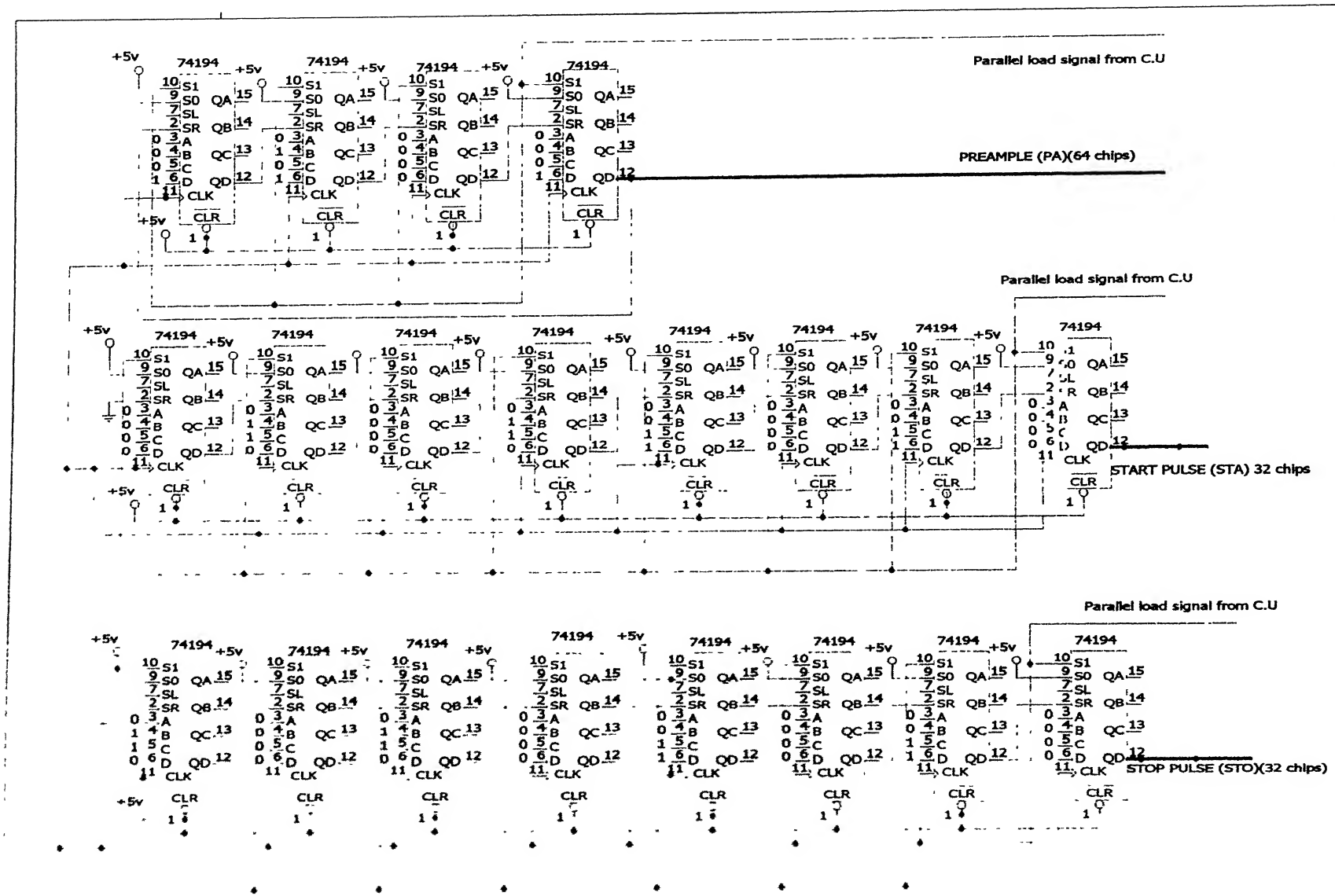


Fig 4 2. PREAMPLE, STA and STO PATTERN GENERATOR

so that chips and symbols on the left are transmitted first [7]. The 32 chip STA pattern was 0000 1100 0000 1100 0110 0000 0110 0000. This was implemented with the help of eight universal shift registers-74LS194. In the transmitting packet of 256 chips, these 32 chips were transmitted from clock numbers 41H to 60H. So a parallel load signal was derived from clock number 40H from the master clock generator, and was provided to the mode selection input (S_1) of all the eight shift registers. Then at the clock number 41H this pattern was loaded parallelly. From next clock onwards this group of four shift registers worked in right shift, serial out mode as shown in Fig. 4.2. Then 32 chips of the STA were generated by 32 shifting operations in this group of eight 74LS194 cascaded in right shift, serial out mode.

c) STOP FLAG

The stop flag (STO) consists of exactly one transmission of the following stream of symbols. In the STO field, the transmission time increases from left to right so that chips and symbols on the left are transmitted first [7]. The 32 chip STO pattern was 0000 1100 0000 1100 0000 0110 0000 0110. This was implemented with the help of eight universal shift registers-74LS194. In the transmitting packet of 256 chips, these 32 chips were transmitted from clock numbers E1H to FFH. So a parallel load signal was derived from clock number E0H from the master clock generator, and it was applied to the mode selection input (S_1) of all the eight shift registers. Then at clock number E1H this pattern was parallelly loaded. From next clock onwards this group of four shift registers works in right shift, serial out mode as shown in Fig. 4.2. Thus 32 chips of the STO was generated by 32 shifting operation in this group of eight 74LS194 cascaded in right shift, serial out mode.

4.1.3 FIR DATA WRAPPER

FIR data wrapper consists of a control logic circuit, which will control flow of 256 chips consists of PA, STA, encoded data and STO one after other as per IrDA FIR standard. The control logic basically consists of an 8-bit master counter and some decoding logic as given in Fig.4.3.

Nature of the Chip	No. Of chips	Original length of Data before encoding	Clock No. used	Signal (Ck. No.) used for parallel load or chip enable	Signal (Ck. No.) used for output enable	Signal (Ck. No.) used for output disable
Pre-Ample	(16X4) =64		1 to 64	00H	00H	40H
Start Pulse	32		65 to 96	40H	40H	60H
* Data	64	32 bits	97 to 224	60H	60H	E0H
** CRC		32 bits				
Stop Pulse	32		225 to 256	E0H	E0H	00H or ***TC)

* 4PPM encoding of 32 bits of data, will provide 64 chips

** If CRC (cyclic redundancy check) is not implemeted then data length will be 64 bits, after encoding it will be 128 chips.

NOTE: In this experimental study CRC is not implemented instead another 32 bits of data was sent during that time.

*** TC means terminal count signal from eight-bit counter.

Fig. 4.3 Decoding Scheme

The eight bit master counter was implemented by cascading two four bit synchronous counters using 74LS163. With the help of 4 input NOR gate (74LS25) and two input AND gate (74LS08) combination, various counts were decoded for generating control signals as shown in Fig. 4.4. Such decoded counts were provided to JK flip-flops implemented using 74LS109. Such four JK flip-flops were used in obtaining the control logic. The first JK flip flop was set using the signal derived from count 00H and it was reset by the count 40H. The output from this JK flip-flop gated PA to the input of the optical transmitter with the help of AND gate and OR gate combination during the clock 01H to 40H. Similarly second JK flip-flop was set using the signal derived from count 40H

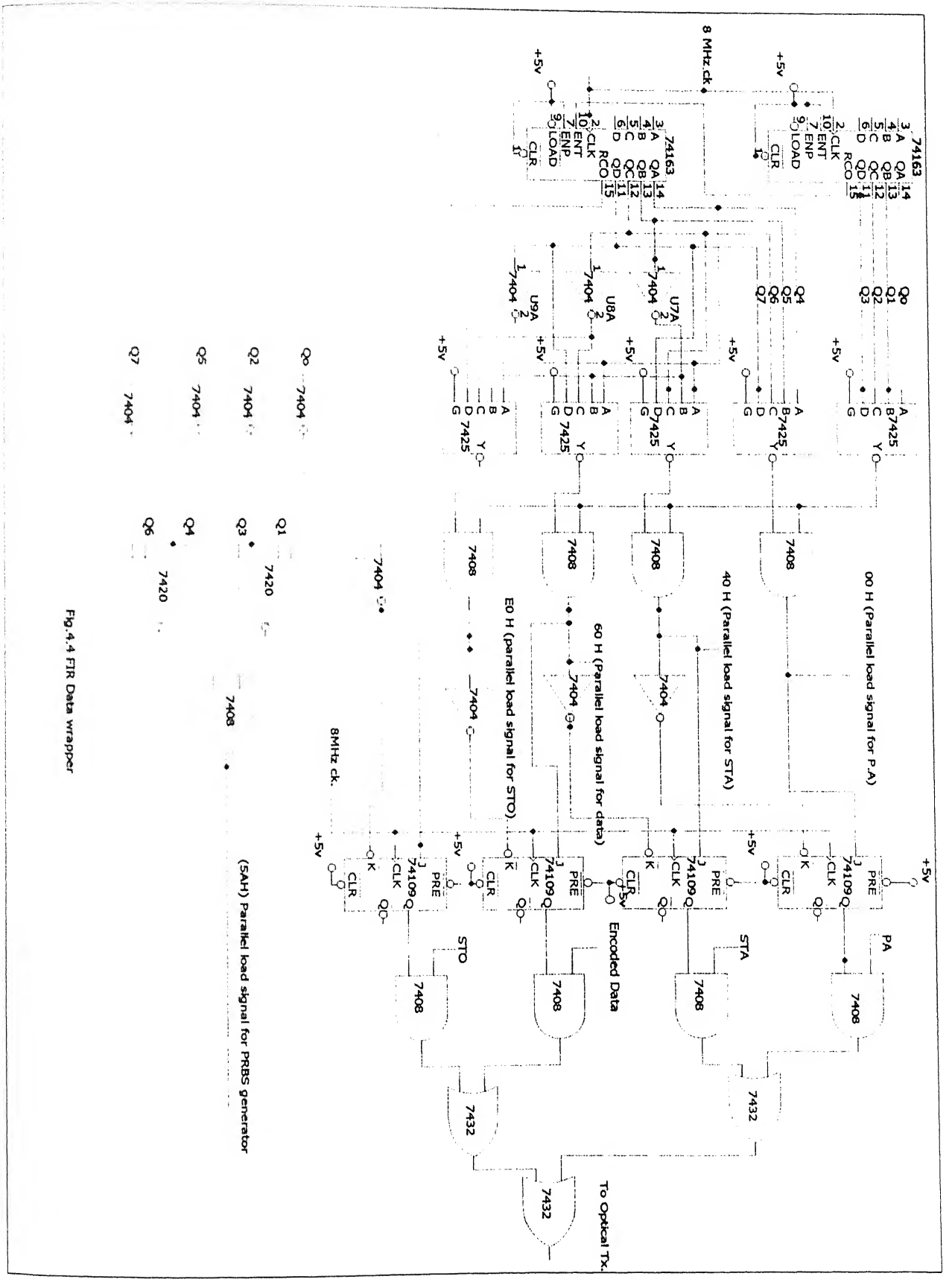


Fig.4.4 FIR Data wrapper

and it was reset by the count 60H. The output from this JK flip-flop gated STA to the input of the optical transmitter with the help of AND gate and OR gate combination during the clock 41H to 60H. The third JK flip flop was set using the signal derived from count 60H and it was reset by the count E0H The output from this JK flip flop gated encoded data from 4PPM data encoder to the input of the optical transmitter with the help of AND gate and OR gate combination during the clock 61H to E0H. The fourth JK flip flop was set using the signal derived from count E0H and it was reset by the count 00H or TC (terminal count) signal from the counter. The output from this JK flip flop gated STO to the input of the optical transmitter with the help of AND gate and OR gate combination during the clock E1H to 00H or up to TC (terminal count) signal from eight bit counter. Thus data is wrapped into a packet of 256 chips with the help above described control logic.

For the proper synchronization of the 4PPM encoder this control logic simultaneously derived a signal from the count 5AH. For parallel loading, derived signals from the count 00H, 40H and E0H are used as parallel load signals for PA, STA and STO pattern generators respectively.

4.1.4 FIR OPTICAL TRANSMITTER

The function of the driver circuit is to supply the necessary drive current to the source LED to turn it on and off in accordance with the data stream presented at the input. Driver circuits capable of handling data rates in excess of 8Mb/s were developed and tested using 830 nm LED [26]. The circuit diagram of the LED driver circuit developed for 830 nm LED source is given in Fig.4. 4.

A single gate of 74S140 driver can source 40mA and sink 68mA, which is quite large for most of the applications. LED is turned ON when the 74S140 gates output is low. In the sink mode the drop across the LED and resistance worked out to be V_{cc}- V_{oL} = 5V-0.2V = 4.8V. The forward drop across LED was about 1.75V. By using two gates of the driver in parallel a drive current of 80 mA was obtained [1]. The LED ON current supplied by the circuit was about 80 mA, each gate supplying a current of 40 mA. A capacitor of 22nF was chosen as speed up capacitor after observing the pulse response.

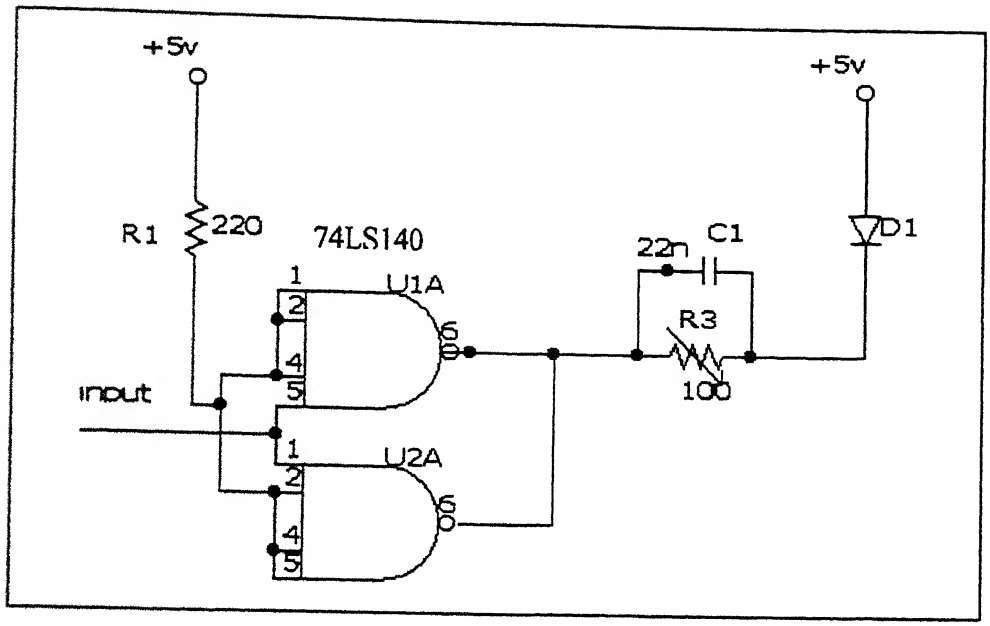


Fig.4.5 LED Transmitter Circuit

Brief specification of the driver circuit is given below.

- Input signal format : TTL, NRZ
- Data rate : 8 Mb/s
- LED wavelength : 830 nm
- Peak to Peak current through the LED : 120 mA

4.2 FIR RECEIVER

FIR receiver consists of a sensitive FIR optical detector and a preamplifier circuit, bit synchronizer based on digital phase locked loop for the clock recovery and a 4PPM decoder for recovering back the data. Optically transmitted data are received at receiver with the help of a PIN- FET detector circuit. From this recovered signal, clocks are recovered with the help of a digital PLL. The encoded data is recovered back with the help of a 4PPM decoder designed using simple discrete components. The implementation details of each are discussed below.

4.2.1 FIR DETECTOR AND PREAMPLIFIER CIRCUIT

The receiver circuit was based on a silicon PIN photodetector and JFET as the front end-amplifying device. The shunt feedback stage with BJT formed its preamplifier stage and a high gain differential video amplifier, implemented using LM733C, formed its post-amplifier. The BJTs used were from the high frequency N-P-N transistor array CA3127E. The output of the post amplifier was fed to a high-speed comparator implemented using NE 529 to obtain a TTL compatible signal. Finally, this signal was fed to the 74S140 line driver for facilitating 50 ohm driving capability.

The detector used in this circuit is RCA C-30808. A reverse bias voltage of 12V was applied and the detector was connected to a FET front-end transimpedence pre-amplifier. The important parameters of the C-30808 detector are given below.

Dark current	:	20 nA
Radius of the active area	:	1.26 mm
Maximum bias voltage	:	15 V
Responsivity at 820 nm	:	0.6 A/W
Capacitance (typical)	:	5 pF

Due to the smaller active area radius, this detector was well suited for applications up to data rate of several Mb/s. The second stage of the receiver consists of the post amplifier, comparator and the line driver. The preamplifier output of about 160 mV at –28.2 dBm was amplified further using the LM733C video amplifier. Out of the three gain settings of LM733C, viz. 10, 100 and 400, the maximum gain of 400 was chosen. The post amplifier output was fed to the NE529 high-speed comparator to obtain a TTL compatible signal.

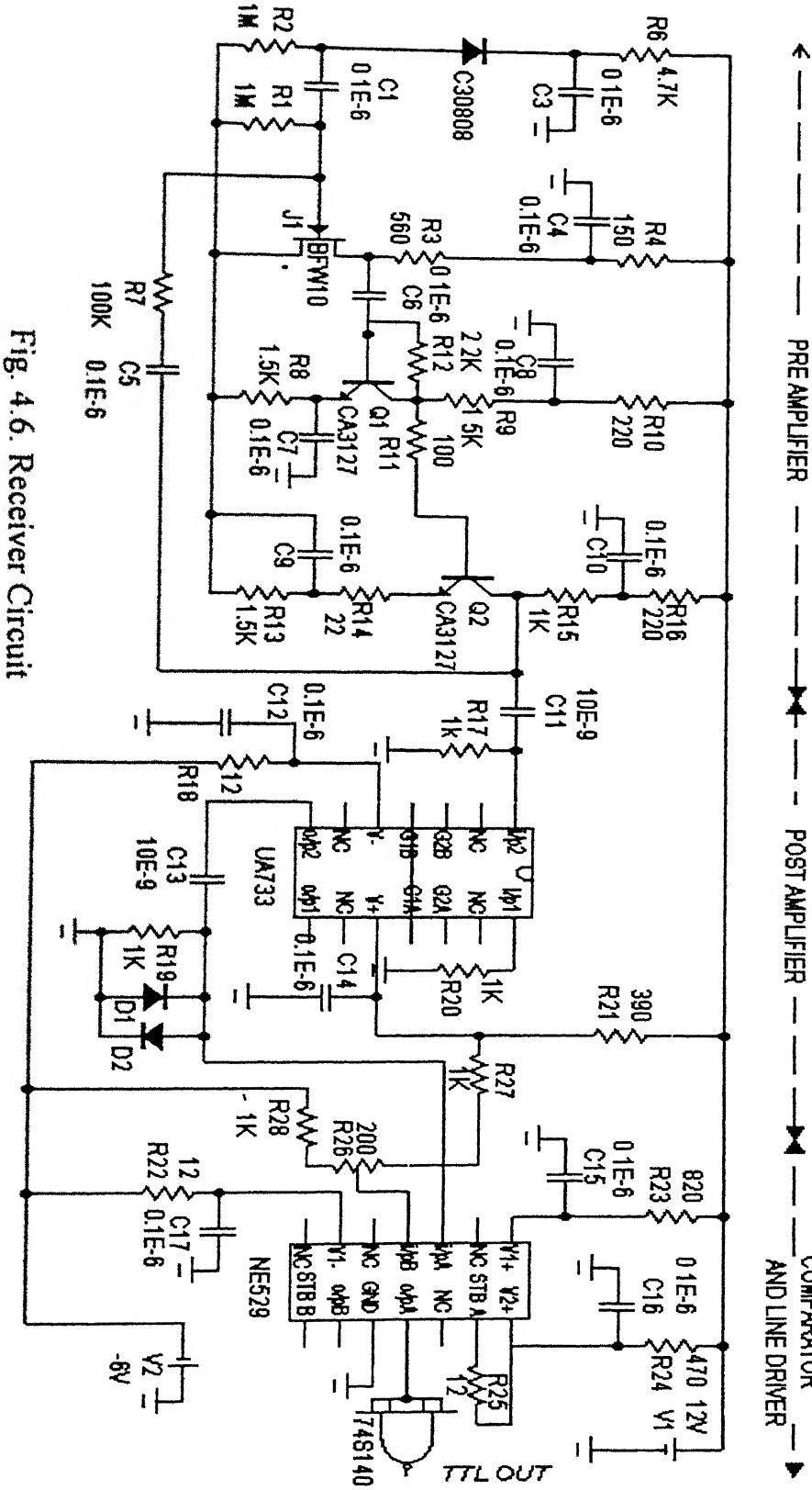


Fig. 4.6. Receiver Circuit

The reference input of the comparator was fine tuned using a resistor network. Finally, this signal was fed to a 74S140 line driver for facilitating 50 ohm driving capability. The obtained values of sensitivity are as follows

Sensitivity of Receiver	= -28.2 dBm at 8 Mb/s,
Peak power	= -28.2 + 3 dBm, (= 2.57 μW)
∴ Peak current, I_p	= 0.6 X 2.57 X 10^{-6} = 1.542 μA.

4.2.2 BIT SYNCHRONISER

Bit synchronizer or the symbol timing recovery scheme is required to extract the timing information or the clock signal from the received non-return to zero (NRZ) bit streams. The symbol timing clock is recovered with the help of a phase locked loop implemented with the help of a digital phase detector and a VCO. Detailed circuit diagram of the bit synchronizer is given in Fig.4.7. The digital phase detector was implemented with the help of Motorola phase frequency detector IC MC4044. MC4044 is an IC consisting basically of three blocks, the phase detector, the charge pump and an amplifier. It contains two phase detectors, phase detector one is based on sequential logic and phase detector two is based on combinational logic. In this implementation phase detector one was used. Since it consists of sequential logic circuitry, the operation prior to lockup was determined by initial conditions. Depending on the phase difference between the inputs, a periodic wave would appear at the up and down outputs of the phase detector. The average value of the resulting waveform was proportional to the phase difference between the two inputs.

The phase detector was implemented by digital phase detector MC4044 and VCO with MC4024. Both of them are linear ICs from Motorola and data sheets are attached in Appendix A. Bit synchronizer was tested with the full system at three frequencies, viz. 2,4 and 6 MHz. In our implementation clock recovery was possible only up to a maximum frequency of 6 MHz. The PLL had too much of jitter at the 8MHz and hence was not useful. The measured capture range at the above frequencies was approximately 100KHz.

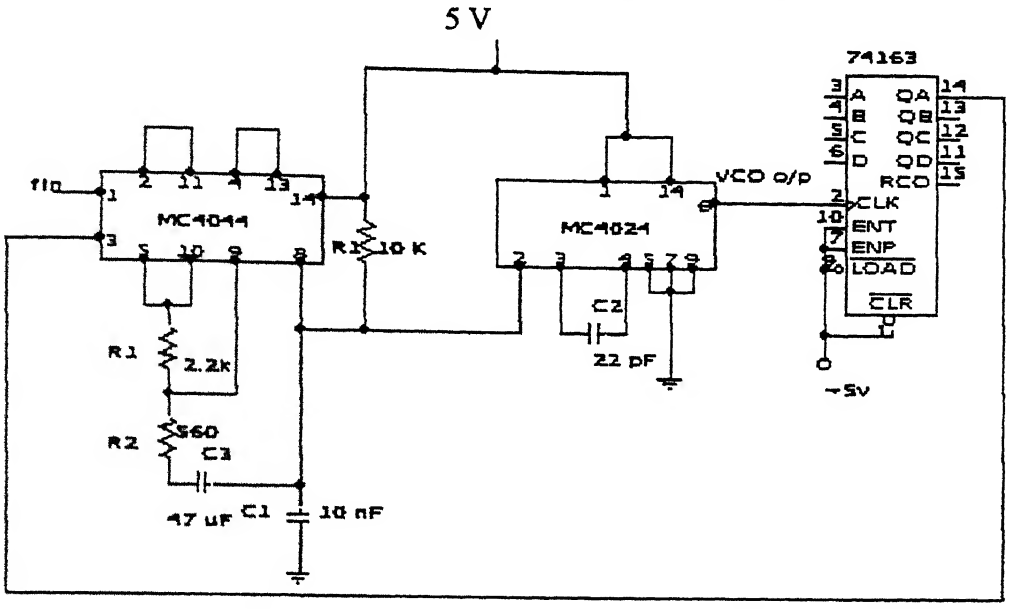


Fig. 4.7 Bit Synchroniser

The capacitance values used in the VCO for the various test frequencies are given below.

C_2	f_0
47 pF	2MHz
22pF	4MHz
10 Pf	6MHz

4.2.3 4PPM DECODER

4PPM decoder would decode the 8 MHz 4PPM encoded data back to 4 MHz data. The detailed circuit diagram is given in Fig.4.8. The 8 MHz encoded chips were received serially and then converted back into cells of 4 such chips using a serial to 4 bit parallel converter. Serial to parallel converter was implemented by 74LS164 serial to parallel converter. The clock signal of 8 MHz.was fed through an AND gate which was controlled by a signal from JK flip-flop which was set by the count 60H and reset by the count E0H.

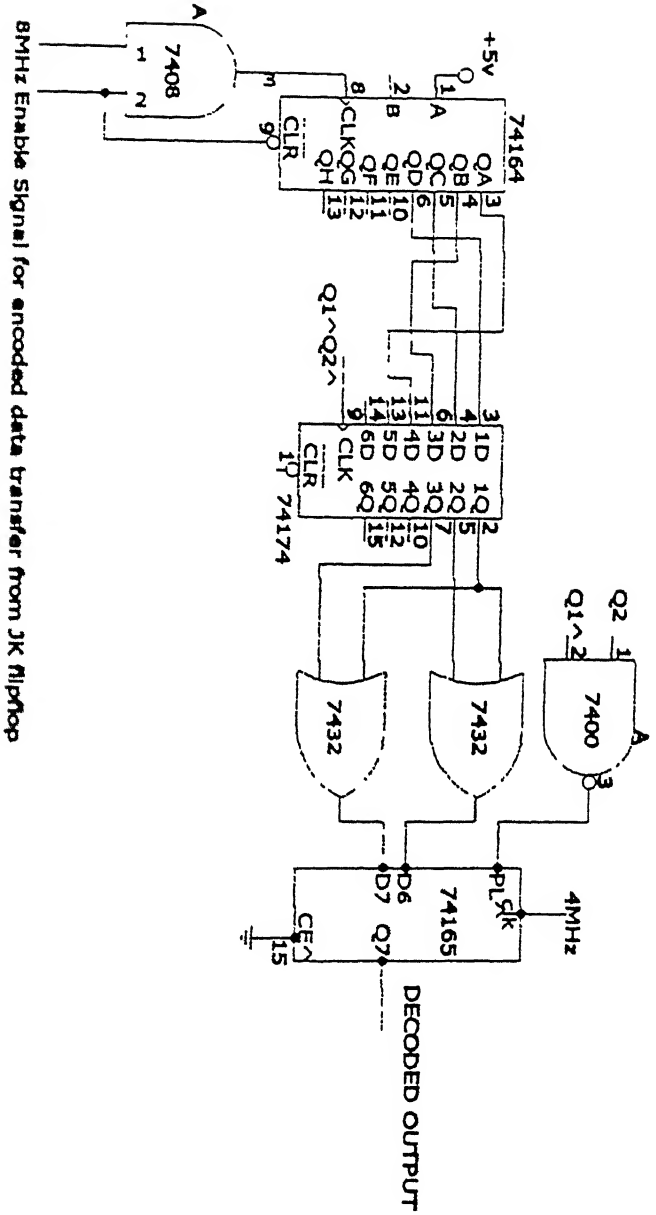


Fig.4.8 4PPM Decoder

The same enable signal from JK flip-flop was provided to the chip enable of 74LS164 so that 4PPM decoder would receive only 128 chips of 4PPM-encoded data from the packetized 256 chips. The output of the serial to parallel converter was sampled by a sampler implemented by 74LS174 D latches at a rate of 2 MHz The 2MHz clock signal was provided from $\overline{Q_1}\,\overline{Q_2}$ to 74LS174 so that proper synchronization could be achieved The 4 bits output from the sampler was provided to a 4:2 decoder. Let A and B be the MSB and LSB of the decoded output and $Y_3Y_2Y_1Y_0$ the inputs. Then 4:2 decoder works based on following equations.

$$A = Y_0 + Y_1$$

$$B = Y_0 + Y_2$$

It was implemented with OR gates 74LS32. This parallel data was converted back in to serial form with the help of a parallel to serial converter implemented by 74LS165 clocked at a frequency of 4 MHz. Thus 4PPM data was decoded back.

4.3 FABRICATION ON A PRINTED CIRCUIT BOARD

The FIR transmitter and receiver circuits were fabricated on a printed circuit board (PCB). The main problems, which can come up in a PCB design, are reflections, cross talk, ground and supply line noise and EMI from pulse type EM field. Hence the following high frequency design rules were kept in mind while preparing the layout of the PCB.

- Length and width of signal conductor should be as small as possible.
- The signal and ground conductors should not be too close as this capacitance along with the output resistance acts as LPF.
- Proximity of input and output conductors should be avoided as this would lead to Miller effect.
- Cross talk could occur if two signal lines run parallel to each other for a length more than 10 cm.
- Measures to reduce ground and supply line noise are to have low impedance between the supply line and the ground line by having broad conductors close to each other. Also, an electro magnetically stable ground, having large copper surface could reduce the noise

- Mains filtering and providing separate shielding could reduce the EMI from pulse type EM fields.

The whole assembly of optical receiver and pre amplifier were shielded using a mild steel box, which enhanced the performance of the receiver by at least 2 dB, and also the output was much more stable.

CHAPTER 5
SUMMARY AND CONCLUSION

The major aims of the work were to study indoor FIR optical wireless systems and to design and implement an experimental IrDA compatible FIR indoor point-to-point link. An extensive review on indoor optical wireless systems was also carried out. A 4 Mb/s indoor FIR wireless optical link has been successfully implemented using discrete components available in laboratory, which is capable of communicating at a distance of 16 cm apart.

The main reason for reduction in sensitivity is believed to be due to noise introduced by ambient light conditions. Another reason may be due to the lack of optimum adjustment in rise time and fall times of the LED transmitter circuit, as a result of which the performance of the overall system was affected. From experiments conducted it was also found that the same receiver would receive data more efficiently if low cost LDs replaced the LED transmitter. However, the LD source was not used due to safety considerations. This point is highlighted to show that if efficiency of the transmitting circuit is increased somehow, better performance can be achieved from the same set up. Use of a better source or concentrators at the receiver end to focus the beam on to the detector, can help in achieving the target of more distance.

The LED transmitter gave an average power output of –4.6 dBm at the transmitter end. The receiver sensitivity was –28.2 dBm at 8Mb/s. The implemented system (4PPM encoder, transmitter, receiver and 4PPM decoder) was capable of a data rate of 4 Mb/s when the same clock was used at the encoder and the decoder. This corresponds to an encoded data rate of 8 Mb/s due to the encoding. The above system however had a slightly inferior performance (a data rate of 3 Mb/s and hence

an encoded data rate of 6 Mb/s) when the decoder used the clock recovered by the bit synchroniser.

Results of the optical link are tabulated in Table 5.1.

Sl No	PARAMETER	TARGET SPECIFIED	TARGET ACHIEVED
1	Bit rate	8 Mb/s	8 Mb/s
2	Distance	>20cm	16 cm
3	BER	$<10^{-9}$	$<10^{-9}$
4	Receiver sensitivity	Better than -30 dBm	-28.2 dBm
5	Dynamic range	10 dB	8.2dB
6	Cost	Moderate	Low cost (used only discrete components available in the lab)
7	Reliability	High	Medium
8	Circuit complexity	Simple	Simple
8	Time for development	< 6 months	6 months

Table 5.1 Summary of target specified and achieved.

From the basis of our study on indoor point-to-point links it can be concluded that these systems are ideally suited for high speed, flexible indoor data transmission.

RECOMMENDATIONS FOR FUTURE WORK

Improvement that can be done to the present system are

1) Use of filters to reduce ambient light at the receiving end.

2) Use of concentrators (lenses) at the receiver end to nullify the effect of beam divergence and thus reduce geometrical spreading loss.

3) Possibility of increasing the power output of the transmitter by power combining of the a few transmitter sources.

5) Instead of a fixed threshold comparator used in the receiver circuit, the use of a peak detector and summing amplifier circuit to facilitate adaptive threshold

7) A better bit synchroniser scheme to improve the clock recovery performance.

MOTOROLA

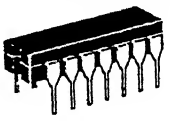
MC4344
MC4044

PHASE-FREQUENCY DETECTOR

The MC4344/4044 consists of two digital phase detectors, a charge pump, and an amplifier. In combination with a voltage controlled multivibrator (such as the MC4324/4024 or MC1648), it is useful in a broad range of phase-locked loop applications. The circuit accepts TTL waveforms at the R and V inputs and generates an error voltage that is proportional to the frequency and/or phase difference of the input signals. Phase detector #1 is intended for use in systems requiring zero frequency and phase difference at lock. Phase detector #2 is used if quadrature lock is desired. Phase detector #2 can also be used to indicate that the main loop, utilizing phase detector #1, is out of lock.

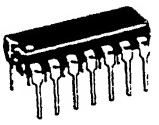
Operating Frequency = 8 MHz typ
Input Loading Factor: R, V = 3
Output Loading Factor (Pin 8) = 10
Total Power Dissipation = 85 mW typ·pkg
Propagation Delay Time = 9.0 ns typ
(thru phase detector)

PHASE-FREQUENCY DETECTOR

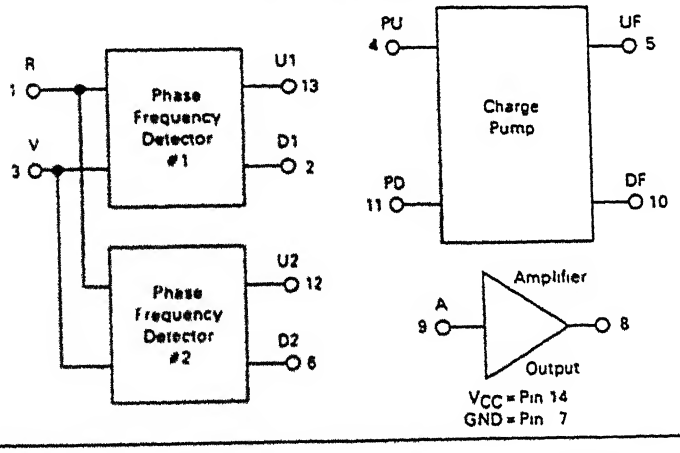


L SUFFIX
CERAMIC PACKAGE
CASE 632
(TO-116)

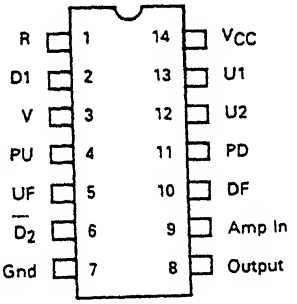
P SUFFIX
PLASTIC PACKAGE
CASE 646
MC4044 only



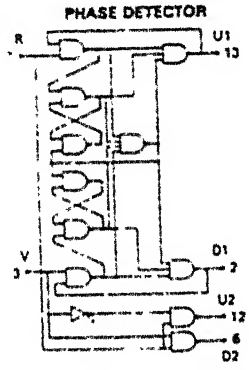
LOGIC DIAGRAM



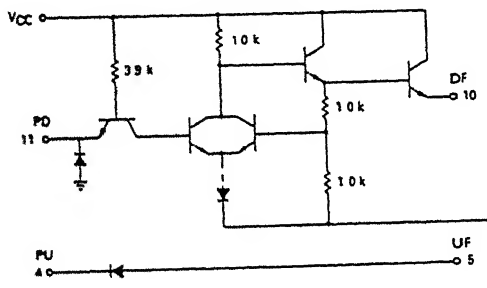
PIN ASSIGNMENT



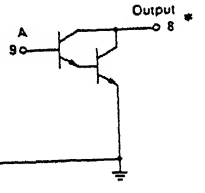
PHASE DETECTOR



CHARGE PUMP

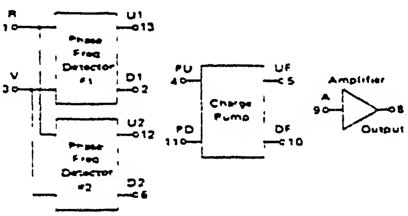


AMPLIFIER



*VMAX not to exceed 8.0 Vdc

ELECTRICAL CHARACTERISTICS



INPUT STATE	INPUT R	INPUT V	OUTPUT U1	OUTPUT D1	OUTPUT U2	OUTPUT D2
1	0	0	X	X	1	1
2	1	0	X	X	0	1
3	1	1	X	X	1	0
4	1	0	X	X	0	1
5	0	0	X	X	1	1
6	1	0	X	X	0	1
7	0	0	0	1	1	1
8	1	0	0	1	0	1
9	0	0	0	1	1	1
10	0	1	0	1	1	1
11	0	0	1	1	1	1
12	0	1	1	1	1	1
13	0	0	1	0	1	1
14	0	1	1	0	1	1
15	0	0	1	0	1	1
16	1	0	1	0	0	1
17	0	0	1	1	1	1

TRUTH TABLE

This is not strictly a functional truth table, i.e., it does not show all possible modes of operation. It is useful for dc testing.

1. X indicates output state unknown
2. U1 and D1 outputs are sequential, i.e., they must be sequenced in order shown
3. U2 and D2 outputs are combinational, i.e., they need only inputs shown to obtain outputs

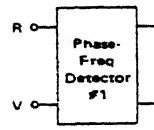
Characteristic	Symbol	Pin Under Test	MC4344 −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC4044 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Input Forward Current	I_F	1		−4.8		−4.8		−4.8		−4.8		−4.8		−4.8	mAdc
		3		−4.8		−4.8		−4.4		−4.8		−4.8		−4.8	
		11		−1.6		−1.6		−1.6		−1.6		−1.6		−1.6	
Leakage Current	I_R	1		[illegible]		120		[illegible]		120		120		120	μAdc
		3		120		120		120		120		120		120	
		4		5.0		5.0		5.0		5.0		5.0		5.0	
		11		40		40		40		40		40		40	
	[illegible]	1				1.0						1.0			mAdc
		3													
Clamp Voltage	V_D	1				−1.5						−1.5			Vdc
		3				−1.5						−1.5			Vdc
Output Voltage (Note 1)	V_{OH}	6	2.4		2.4		2.4		2.5		2.5		2.5		Vdc
		12	2.4		2.4		2.4		2.5		2.5		2.5		Vdc
	V_{OL}	6		0.4		0.4		0.4		0.4		0.4		0.4	Vdc
	V_{OH}	12	2.4		2.4		2.4		2.5		2.5		2.5		Vdc
	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	Vdc
	V_{OL}	2		0.4		0.4		0.4		0.4		0.4		0.4	Vdc
	V_{OH}	13	2.4		2.4		2.4		2.5		2.5		2.5		Vdc
	V_{OL}	2		0.4		0.4		0.4		0.4		0.4		0.4	Vdc
	V_{OH}	13	2.4		2.4		2.4		2.5		2.5		2.5		Vdc
	V_{OL}	2		0.4		0.4		0.4		0.4		0.4		0.4	Vdc
	V_{OH}	13	2.4		2.4		2.4		2.5		2.5		2.5		Vdc
	V_{OH}	2	2.4		2.4		2.4		2.5		2.5		2.5		Vdc
		13	2.4		2.4		2.4		2.5		2.5		2.5		Vdc
Short-Circuit Current (Note 1)	I_{OS}	2, 6, 12, 13	20	−65	20	65	20	65	20	65	20	−65	20	−65	mAdc
Leakage Current (Note 1)	I_{CEX}	2, 6, 12, 13		250		250		250		250		250		250	μAdc
Diode Voltage	V_F	5			0.5						0.5				Vdc
Output Voltage	V_{EN}	10	1.5		1.5		1.5		1.5		1.5		1.5		Vdc
Output Current	I_O	8	0.2		0.8		1.0		0.5		0.8		1.0		mAdc
Leakage Current	I_{OLK}	8		120		120		120		120		120		120	μAdc
		10		5.0		5.0		5.0		5.0		5.0		5.0	μAdc
Power Requirements (Total Device) Power Supply Drain	I_{CC}	14		40		40		40		40		40		40	mAdc

APPLICATION

Operation of the MC4344/4044 is best explained by initially considering each section separately. If phase detector #1 is used, loop lockup occurs when both outputs U1 and D1 remain high. This occurs only when all the negative transitions on R, the reference input, and V, the variable or feedback input, coincide. The circuit responds only to transitions, hence phase error is independent of input waveform duty cycle or amplitude variation. Phase detector #1 consists of sequential logic circuitry, therefore operation prior to lockup is determined by initial conditions.

When operation is initiated, by either applying power to the circuit or active input signals to R and V, the circuitry can be in one of several states. Given any particular starting conditions, the flow table of Figure 1 can be used to determine subsequent operation. The flow table indicates the status of U1 and D1 as the R and V inputs are varied. The numbers in the table which are in parentheses are arbitrarily assigned labels that correspond to stable states that can result for each input combination. The numbers without parentheses refer to unstable conditions. Input changes are traced by horizontal movement in the table; after each input change, circuit operation will settle in the numbered state indicated by moving horizontally to the appropriate R-V column. If the number at that location is not in parentheses, move vertically to the number of the same value that is in parentheses. For a given input pair, any one of three stable states can exist. As an example, if R = 1 and V = 0, the circuit will be in one of the stable states (4), (8), or (12).

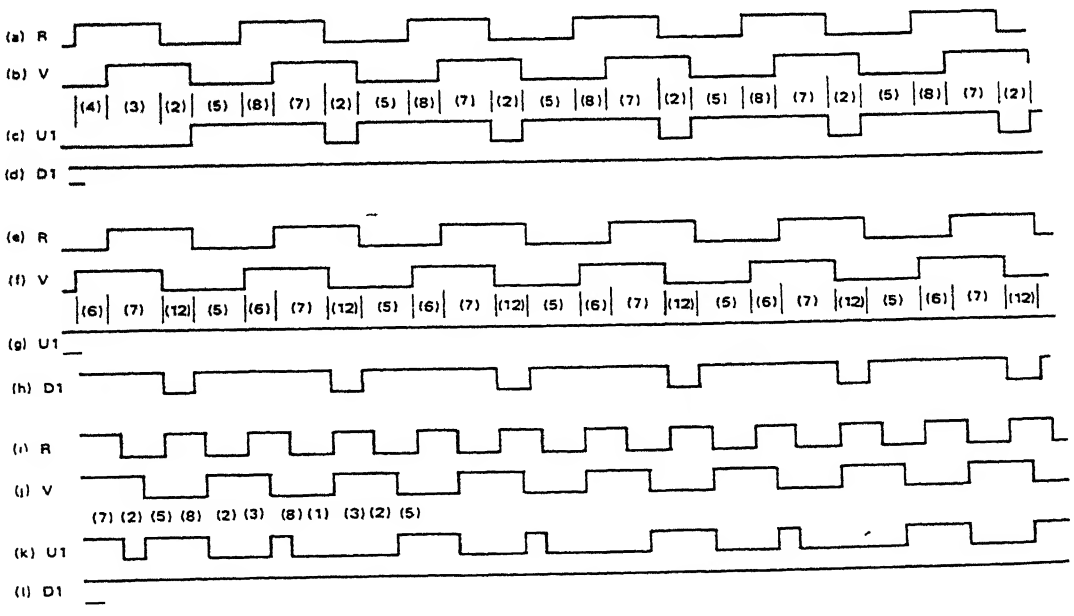
FIGURE 1 — PHASE DETECTOR #1 FLOW TABLE



R-V 0-0	R V 0 1	R-V 1-1	R-V 1-0	U1	D1
(1)	2	3	(4)	0	1
5	(2)	(3)	8	0	1
(5)	6	7	8	1	1
9	(6)	7	12	1	1
5	2	(7)	12	1	1
5	2	7	(8)	1	1
(9)	(10)	11	12	1	0
5	6	(11)	(12)	1	0

Use of the table in determining circuit operation is illustrated in Figure 2. In the timing diagram, the input to R is the reference frequency; the input to V is the same frequency but lags in phase. Stable state (4) is arbitrarily assumed as the initial condition. From the timing diagram and flow table, when the circuit is in stable state (4), outputs U1 and D1 are "0" an "1" respectively. The next input state is R-V = 1-1; moving horizontally from stable state (4) under R-V = 1-0 to the R-V = 1-1 column, state 3 is indicated. However, this is an unstable condition and the circuit will assume the state indicated by moving vertically in the R-V = 1-1 column to stable state (3). In this

FIGURE 2 — PHASE DETECTOR #1 TIMING DIAGRAM



instance, outputs U1 and D1 remain unchanged. The input states next become R-V = 0-1, moving horizontally to the R-V = 0-1 column, stable state (2) is indicated. At this point there is still no change in U1 or D1. The next input change shifts operation to the R-V = 0-0 column where unstable state 5 is indicated. Moving vertically to stable state (5), the outputs now change state to U1-D1 = 1-1. The next input change, R-V = 1-0, drives the circuitry to stable state (8), with no change in U1 or D1. The next input, R-V = 1-1, leads to stable state (7) with no change in the outputs. The next two input state changes cause U1 to go low between the negative transitions of R and V. As the inputs continue to change, the circuitry moves repeatedly through stable states (2), (5), (8), (7), (2), etc., as shown, and a periodic waveform is obtained on the U1 terminal while D1 remains high.

A similar result is obtained if V is leading with respect to R, except that the periodic waveform now appears on D1 as shown in rows e–h of the timing diagram of Figure 2. In each case, the average value of the resulting waveform is proportional to the phase difference between the two inputs. In a closed loop application, the error signal for controlling the VCO is derived by translating and filtering these waveforms.

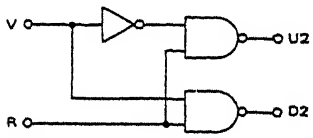
The results obtained when R and V are separated by a fixed frequency difference are indicated in rows i–l of the timing system. For this case, the U1 output goes low when R goes low and stays in that state until a negative transition on V occurs. The resulting waveform is similar to the fixed phase difference case, but now the duty cycle of the U1 waveform varies at a rate proportional to the difference frequency of the two inputs, R and V. It is this characteristic that permits the MC4344/4044 to be used as a frequency discriminator; if the signal on R has been frequency modulated and if the loop bandwidth is selected to pass the deviation frequency but reject R and V, the resulting error voltage applied to the VCO will be the recovered modulation signal.

Phase detector #2 consists only of combinatorial logic, therefore its characteristics can be determined from the simple truth table of Figure 3. Since circuit operation requires that both inputs to the charge pump either be high or have the same duty cycle when lock occurs, using this phase detector leads to a quadrature relationship between R and V. This is illustrated in rows a–d of the timing diagram of Figure 3. Note that any deviation from a fifty percent duty cycle on the inputs would appear as phase error.

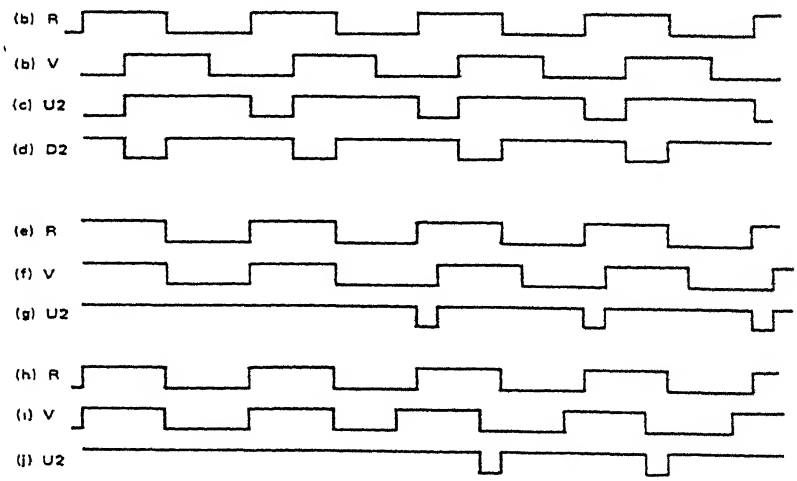
Waveforms showing the operation of phase detector #2 when phase detector #1 is being used in a closed loop are indicated in rows e–j. When the main loop is locked, U2 remains high. If the loop drifts out of lock in either direction a negative pulse whose width is proportional to the amount of drift appears on U2. This can be used to generate a simple loss-of-lock indicator.

Operation of the charge pump is best explained by considering it in conjunction with the Darlington amplifier included in the package (see Figure 4). There will be

FIGURE 3 — PHASE DETECTOR #2 OPERATION

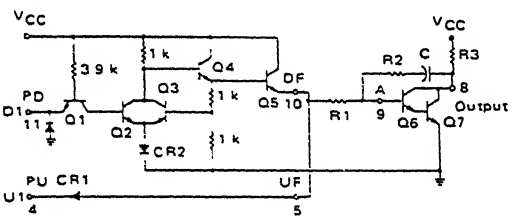


R	V	U2	D2
0	0	1	1
0	1	1	1
1	0	0	1
1	1	1	0



a pulsed waveform on either PD or PU, depending on the phase-frequency relationship of R and V The charge pump serves to invert one of the input waveforms (D1) and translates the voltage levels before they are applied to the loop filter When PD is low and PU is high, Q1 will be conducting in the normal direction and Q2 will be off Current will be flowing through Q3 and CR2, the base of Q3 will be two V_{BE} drops above ground or approximately 1.5 volts Since both of the resistors connected to the base of Q3 are equal, the emitter of Q4 (base of Q5) will be approximately 3 0 volts For this condition, the emitter of Q5 (DF) will be on V_{BE} below this voltage, or about 2.25 volts The PU input to the charge pump is high (> 2 4 volts) and CR1 will be reverse biased. Therefore Q5 will be supplying current to Q6 This will tend to lower the voltage at the collector of Q7, resulting in an error signal that lowers the VCO frequency as required by a "pump down" signal

FIGURE 4 — CHARGE PUMP OPERATION

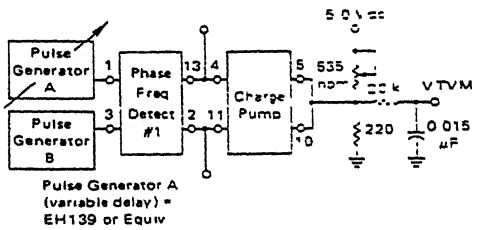


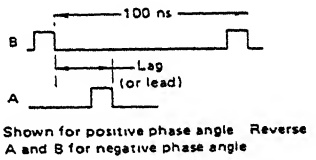
When PU is low and PD is high, CR1 is forward biased and UF will be approximately one V_{BE} above ground (neglecting the $V_{CE(sat)}$ of the driving gate). With PD high, Q1 conducts in the reverse direction, supplying base current for Q2. While Q2 is conducting, Q4 is prevented from supplying base drive to Q5, with Q5 cut off and UF low there is no base current for Q6 and the voltage at the collector of Q7 moves up, resulting in an increase in the VCO operating frequency as required by a "pump up" signal.

If both inputs to the charge pump are high (zero phase difference), both CR1 and the base-emitter junction of Q5 are reverse biased and there is no tendency for the error voltage to change. The output of the charge pump varies between one V_{BE} and three V_{BE} as the phase difference of R and V varies from minus 2π to plus 2π If this signal is filtered to remove the high-frequency components, the phase detector transfer function, K_ϕ, of approximately 0.12 volt/radian is obtained (see Figure 5).

The specified gain constant of 0 12 volt/radian may not be obtained if the amplifier/filter combination is improperly designed As indicated previously, the charge pump delivers pump commands of about 2.25 volts on the positive swings and 0.75 volt on the negative swings for a mean no-pump value of 1 5 volts If the filter amplifier is biased to threshold "on" at 1.5 volts, then the pump up and down voltages have equal effects The pump signals are established by V_{BE}s of transistors with milliamperes of current flowing. On the other hand, the transistors included for use as a filter amplifier will have very small currents flowing and will have correspondingly lower V_{BE}s — on the order of 0.6 volt each for a threshold of 1.2 volts. Any displacement of the threshold from 1.5 volts causes an increase in gain in one direction and a reduction in the other. The transistor configuration provided is hence not optimum but does allow for the use of an additional transistor to improve filter response. This addition also results in a non-symmetrical response since the threshold is now approximately 1.8 volts The effective positive swing is limited to 0 45 volt while the negative swing below threshold can be greater than 1 0 volt. This means that the loop gain when changing from a high frequency to a lower frequency is less than when changing in the opposite direction. For type two loops this tends to increase overshoot when going from low to high and increases damping in the other direction. These problems and the selection of external filter components are intimately related to system requirements and are discussed in detail in the filter design section.

FIGURE 5 — PHASE DETECTOR TEST





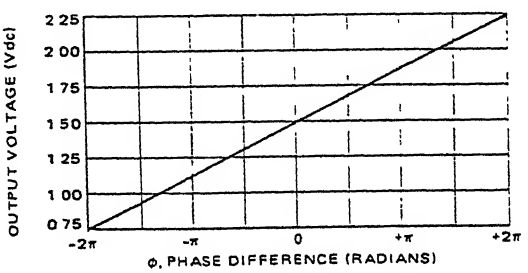


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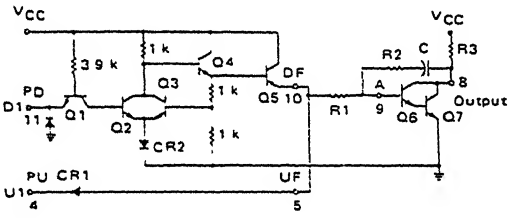
FIGURE 4 — CHARGE PUMP OPERATION



When PU is low and PD is high, CR1 is forward biased and UF will be approximately one V_{BE} above ground (neglecting the $V_{CE(sat)}$ of the driving gate) With PD high, Q1 conducts in the reverse direction, supplying base current for Q2. While Q2 is conducting, Q4 is prevented from supplying base drive to Q5, with Q5 cut off and UF low there is no base current for Q6 and the voltage at the collector of Q7 moves up, resulting in an increase in the VCO operating frequency as required by a "pump up" signal.

With both inputs to the charge pump at high (zero phase difference), both CR1 and the base-emitter junction of Q5 are reverse biased and there is no tendency for the error voltage to change The output of the charge pump varies between one V_{BE} and three V_{BE} as the phase difference of R and V varies from minus 2π to plus 2π. If this signal is filtered to remove the high-frequency components, the phase detector transfer function, K_ϕ, of approximately 0.12 volt/radian is obtained (see Figure 5).

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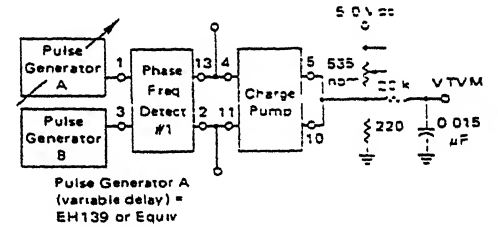
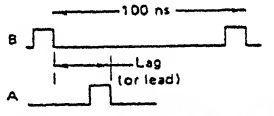
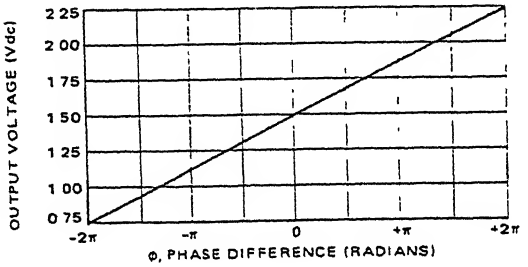
FIGURE 5 — PHASE DETECTOR TEST



Pulse Generator A (variable delay) = EH139 or Equiv



Shown for positive phase angle Reverse A and B for negative phase angle



MOTOROLA

MC4324
MC4024

DUAL VOLTAGE-CONTROLLED MULTIVIBRATOR

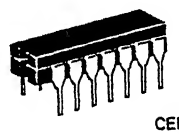
The MC4324/4024 consists of two independent voltage-controlled multivibrators with output buffers Variation of the output frequency over a 3.5-to-1 range is guaranteed with an input dc control voltage of 1 0 to 5 0 voltage

Operating frequency is specified at 25 MHz at 25°C Operation to 15 MHz is possible over the specified temperature range For higher frequency requirements, see the MC1648 (200 MHz) or the MC1658 (125 MHz) data sheet

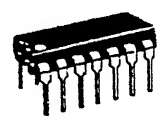
This device was designed specifically for use in phase-locked loops for digital frequency control It can also be used in other applications requiring a voltage-controlled frequency, or as a stable fixed frequency oscillator (3.0 MHz to 15 MHz) by replacing the external control capacitor with a series mode crystal

Maximum Operating Frequency = 25 MHz Guaranteed @ 25°C
Power Dissipation = 150 mW typ pkg
Output Loading Factor = 7

DUAL VOLTAGE-CONTROLLED MULTIVIBRATOR



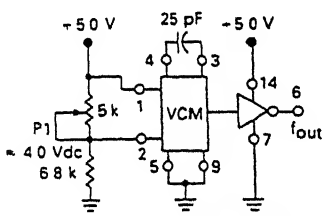
L SUFFIX
CERAMIC PACKAGE
CASE 632
(TO-116)



P SUFFIX
PLASTIC PACKAGE
CASE 646
(MC4024 only)

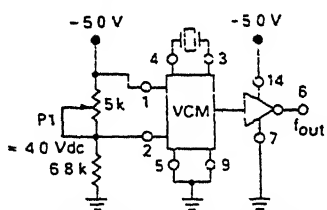
TYPICAL APPLICATIONS

FIGURE 1 — ASTABLE MULTIVIBRATOR



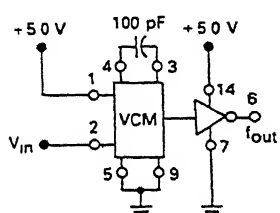
f_{out} = 10 MHz

FIGURE 2 — CRYSTAL CONTROLLED MULTIVIBRATOR



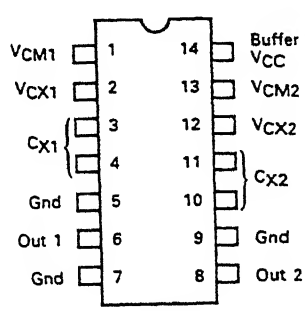
Crystal frequency can be pulled slightly by adjusting P1

FIGURE 3 — VOLTAGE-CONTROLLED MULTIVIBRATOR

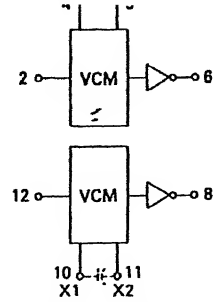


V_{in} = 2 5 V to 5 5 V
f_{out} = 1 0 MHz min, 5 0 MHz max

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

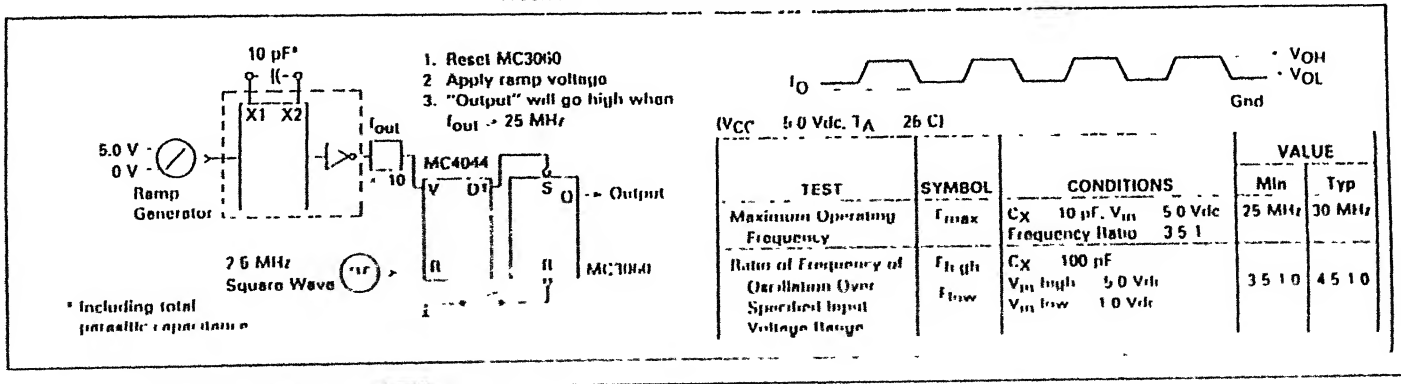


Gnd: VCM = 5, 9
Output Buffer = 7
External Capacitor for Frequency Range Determination

	Test Temperature	TEST CURRENT/VOLTAGE VALUES mA I_{OL1}	I_{OL2}	I_{OH}	Volts V_{IH}	V_{CC}	V_{CCL}	V_{CCH}
MC4324	−55°C	9.8	11.2	−1.6	5.0	5.0	4.5	5.5
	+25°C	9.8	11.2	−1.6	5.0	5.0	4.5	5.5
	+125°C	9.8	11.2	−1.6	5.0	5.0	4.5	5.5
MC4024	0°C	9.8	11.2	−1.6	5.0	5.0	4.75	5.25
	+25°C	9.8	11.2	−1.6	5.0	5.0	4.75	5.25
	+75°C	9.8	11.2	−1.6	5.0	5.0	4.75	5.25

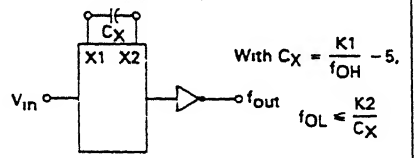
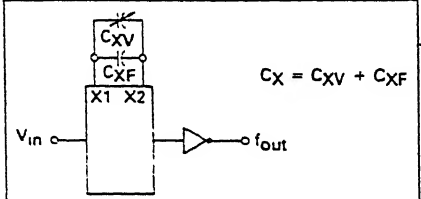
Characteristic	Symbol	Pin Under Test	MC4324 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC4024 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW I_{OL1}	I_{OL2}	I_{OH}	V_{IH}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input Forward Current	I_{in}	2	—	100	—	100	—	100	—	100	—	100	—	100	µAdc	—	—	—	2	—	—	14	5,7,9
		12	—	100	—	100	—	100	—	100	—	100	—	100	µAdc	—	—	—	12	—	—	14	5,7,9
Output Output Voltage	V_{OL}	6	—	0.4	—	0.4	—	0.4	—	0.4	—	0.4	—	0.4	Vdc	8	—	—	2	—	1,4,14	—	5,7,9
		8	—	↓	—	↓	—	↓	—	↓	—	↓	—	↓	↓	8	—	—	12	—	10,13,14	—	↓
		6	—		—		—		—		—		—			—	6	—	2	—	—	1,4,14	
		8	—		—		—		—		—		—			—	8	—	12	—	—	10,13,14	
	V_{OH}	6	2.4	—	2.4	—	2.4	—	2.5	—	2.5	—	2.5	—	Vdc	—	—	6	2	—	1,3,14	—	5,7,9
		8	2.4	—	2.4	—	2.4	—	2.5	—	2.5	—	2.5	—	Vdc	—	—	8	12	—	11,13,14	—	5,7,9
Short-Circuit Current	I_{OS}	6	−20	−65	−20	−65	−20	−65	−20	−65	−20	−65	−20	−65	mAdc	—	—	—	2	1,3,14	—	—	5,6,7,9
		8	−20	−85	−20	−65	−20	−65	20	85	20	−65	20	85	mAdc	—	—	—	12	11,13,14	—	—	5,7,8,9
Power Requirements (Total Device) Power Supply Drain	I_{CC}	1,3,14	—	—	—	37	—	—	—	—	—	37	—	—	mAdc	—	—	—	2,4,10,12	1,13,14	—	—	5,7,9

FIGURE 4 — AC TEST CIRCUIT AND WAVEFORMS



TEST	SYMBOL	CONDITIONS	VALUE Min	VALUE Typ
Maximum Operating Frequency	f_{max}	C_X = 10 pF, V_{in} = 5.0 Vdc, Frequency Ratio = 3.5.1	25 MHz	30 MHz
Ratio of Frequency of Oscillation Over Specified Input Voltage Range	f_{high} / f_{low}	C_X = 100 pF, V_{in} high = 5.0 Vdc, V_{in} low = 1.0 Vdc	3.5.1.0	4.5.1.0

TABLE 1 — EXTERNAL CONTROL CAPACITOR VALUE DETERMINATION

CONFIGURATION	T_A	V_{CC}	VALUES OF K				
			K1	K2	K3	K4	K5
 With $C_X = \frac{K1}{f_{OH}} - 5$, $f_{OL} \leq \frac{K2}{C_X}$	25°C ±3°C	5.0 V	385	150	600	110	1.0
		5.0 V ±5%	325	175	680	125	1.14
		5.0 V ±10%	290	190	750	140	1.25
 $C_X = C_{XV} + C_{XF}$	0°C to 75°C	5.0 V	335	165	660	120	1.10
		5.0 V ±5%	280	190	750	140	1.25
		5.0 V ±10%	250	200	840	150	1.40
Choose C_{XF} and C_{XV} such that C_X can be adjusted to $\frac{K1}{f_{OH}} - 5 \leq C_X \leq \frac{K3}{f_{OH}} - 5$ With $V_{in} = V_{CC} = 5.0$ V, adjust C_X to obtain. $f_{out} = K5\,(f_{OH})$ Then $f_{OL} \leq \frac{K4}{K1} f_{OH}$	−55°C to 125°C	5.0 V	300	175	690	125	1.15
		5.0 V ±5%	260	200	780	145	1.30
		5.0 V ±10%	230	210	860	155	1.45

Definitions f_{OH} = Output frequency with $V_{in} = V_{CC}$
f_{OL} = Output frequency with $V_{in} = 2.5$ V
(Frequencies in MHz, C_X in pF)

value in picofarads to obtain output frequency in megahertz. In Figure 6 the ordinate axis is multiplied by the capacitor value in picofarads to obtain the gain constant (K_V) in radians/second/volt.

Frequency Stability

When the MC4324/4024 is used as a fixed-frequency oscillator (V_{in} constant), the output frequency will vary slightly because of internal noise. This variation is indicated by Figure 10 for the circuit of Figure 11. These variations are relatively independent (< 10%) of changes in temperature and supply voltage.

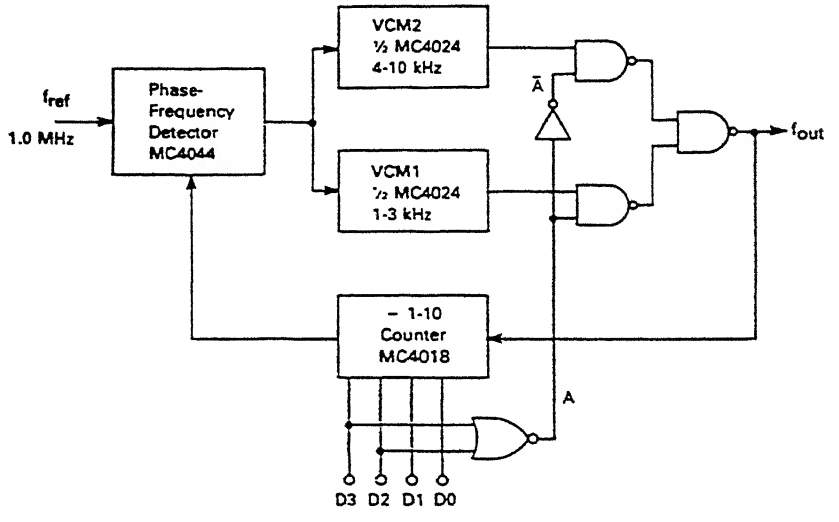
10-to-1 Frequency Synthesizer

A frequency synthesizer covering a 10-to-1 range is shown in Figure 14. Three packages are required to complete the loop. The MC4344/4044 phase-frequency detector, the MC4324/4024 dual voltage-controlled multivibrator, and the MC4318/4018 programmable counter. Two VCM's (one package) are used to obtain the required frequency range. Each VCM is capable of operating over a 3-to-1 range, thus VCM1 is used for the lower portion of the times ten range and VCM2 covers the upper end. The proper divide ratio is set into the programmable counter and the VCM for that frequency is selected by control gates. The other VCM is left to be free running since its output is gated out of the feedback path.

Normally with a single VCM the loop gain would vary over a 10-to-1 range due to the range of the counter ratios. This affects the bandwidth, lockup time, and damping ratio severely. Utilizing two VCM's reduces this change in loop gain rom 10-to-1 to 3-to-1 as a result of the different sensitivities of the two VCM's due to the different frequency ranges. This change of VCM sensitivity (3-to-1) is of such a direction of compensate for loop gain variations due to the programmable counter.

The overall concept of multi-VCM operation can be expanded for ranges greater than 10-to-1. Four VCM's (two packages) could be used to cover a 100-to-1 range.

FIGURE 12 — 10-TO-1 FREQUENCY SYNTHESIZER



÷N	Input D3	D2	D1	D0	A	VCM1 kHz	VCM2 kHz	f_{out} kHz
1	0	0	0	1	1	1	X	1
2	0	0	1	0	1	2	X	2
3	0	0	1	1	1	3	X	3
4	0	1	0	0	0	X	4	4
5	0	1	0	1	0	X	5	5
6	0	1	1	0	0	X	6	6
7	0	1	1	1	0	X	7	7
8	1	0	0	0	0	X	8	8
9	1	0	0	1	0	X	9	9
10	1	0	1	0	0	X	10	10

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